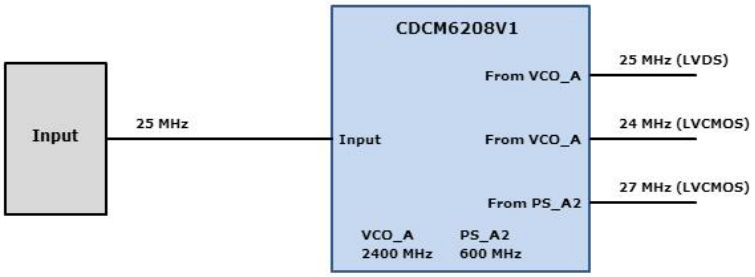
WEBENCH® Clock Architect

Project Report

Project: 4388007/1 Project 1 - [CDCM6208V1]
Created: 6/10/15 1:03:52 AM



Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

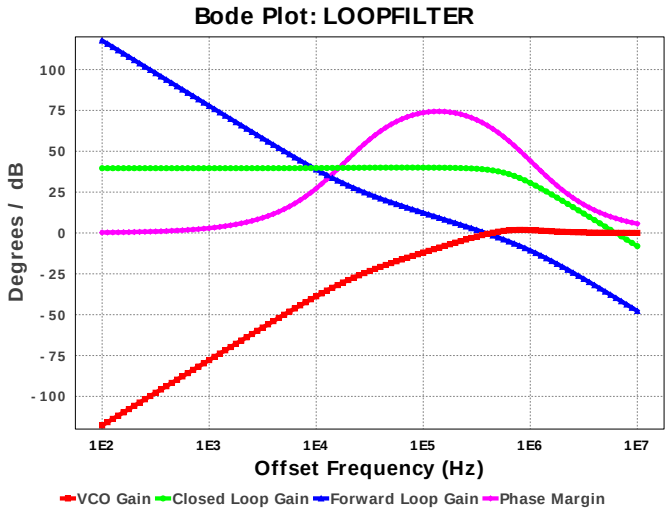
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$5.2
Total Current	137.5 mA
Total Footprint	49.0 mm^2

User ID = 4388007
Design Id = 4
Device = CDCM6208V1
Created = 6/10/15 1:03:52 AM

WEBENCH® Clock Design Report

Loop Filter: LOOPFILTER



Preferences

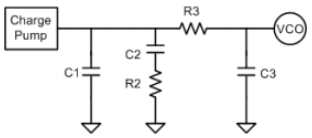
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.50 mA
VCO Gain	185.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	25.00 MHz

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	423.625 kHz	N	382.114 kHz
Phase Margin	65.00 deg	N	66.447 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	9.50	N	7.626

Loop Filter Components

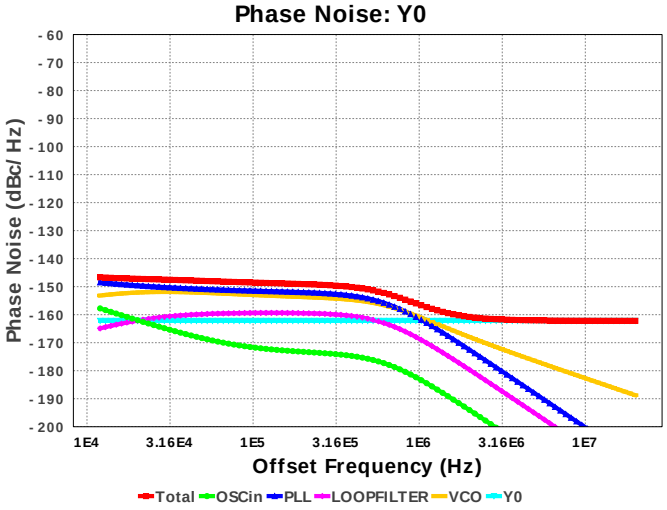
	Name	Target Value	Fixed	Forced
1.	C1	Open	N	N
	C2	15.00 nF	N	N
	C3	0.242 nF	Y	N
4.	C4	Open	Y	N
	R2	0.56 kohms	N	N
	R3	0.10 kohms	Y	N



Output Block: Y0 as LVDS output, 25.0 MHz

Integrated Noise Info

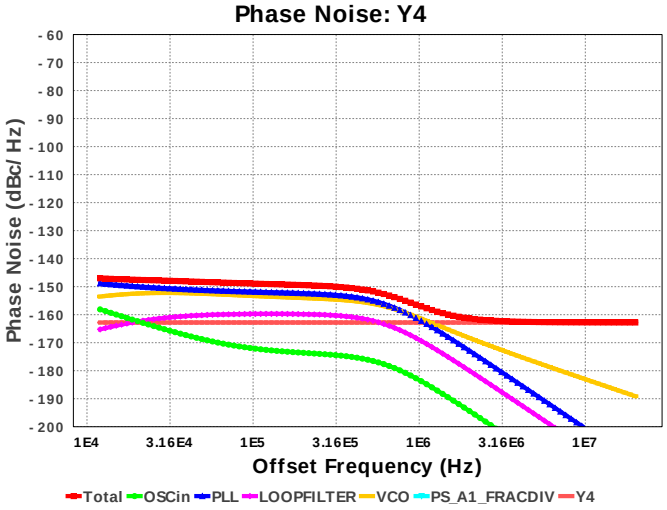
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-159.896 dBc/Hz
RMS Jitter	407.37 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.064 mrad
EVM	0.006%
SNR	83.878 dB
Spur	-86.878 dBc
Jitter (Pk-Pk)	2904.75 fs
Jitter (Cycle to Cycle Pk)	5809.50 fs
Jitter (Cycle to Cycle RMS)	576.108 fs
A/D ENOB	13.647 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: Y4 as LVCMOS output, 24.0 MHz

Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-160.393 dBc/Hz
RMS Jitter	400.732 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.06 mrad
EVM	0.006%
SNR	84.375 dB
Spur	-87.375 dBc
Jitter (Pk-Pk)	2857.421 fs
Jitter (Cycle to Cycle Pk)	5714.841 fs
Jitter (Cycle to Cycle RMS)	566.721 fs
A/D ENOB	13.73 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: Y5 as LVCMOS output, 26+23301686/23301689 MHz

Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-152.499 dBc/Hz
RMS Jitter	883.868 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.15 mrad
EVM	0.015%
SNR	76.481 dB
Spur	-79.481 dBc
Jitter (Pk-Pk)	6302.418 fs
Jitter (Cycle to Cycle Pk)	12604.836 fs
Jitter (Cycle to Cycle RMS)	1249.978 fs
A/D ENOB	12.419 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00