LM3445/48 Phase Dimming Work Book

Longmont Applications Engineering Team **May 20th 2011- Revision 1.0a**

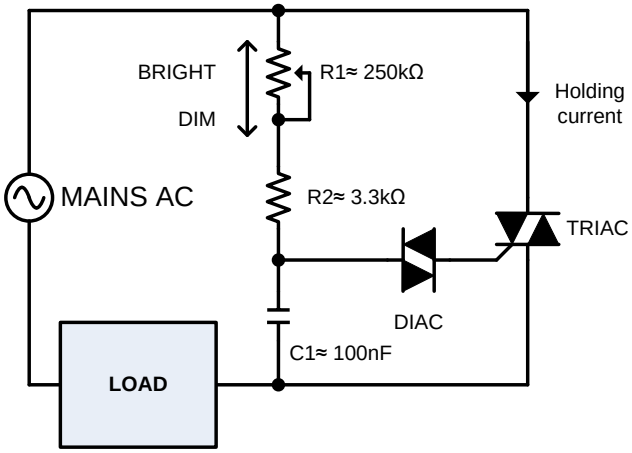
Table of Contents

SSL Phase Dimming, Why

Solid State Lighting (SSL) offers incredible energy savings, and reliability (lifetime) benefits from traditional incandescent, halogen, and fluorescent lighting architectures. SSL fixtures and their light source LEDs require power electronics to regulate, and dim the current through the LED string. Although this is fairly easy to and a well understood science, it is a technology that is not found in the other traditional light sources. Currently there are billions of incandescent bulbs in the world today, and many of these bulbs are dimmed (controlled) with phase dimmers. Phase dimmers were designed to work well with inefficient incandescent bulbs, and are very inexpensive to manufacture due to their simplicity and volume produced each month. With billions of traditional phase dimmers in the world, it is very attractive to try and make SSL type light sources compatible with existing phase dimmers. This is easier said than done. In this workbook I discuss trade-offs, common issues, and methods to resolve these compatibility issues.

Phase Dimmer Basics

Residential dimmers for incandescent bulbs primarily utilize phase modulating dimming through triac switches to control the power sent to the bulb. These dimmers actually control the RMS voltage applied to the bulb by suppressing part of the AC line voltage using a triac. The effect is a chopped sine wave. Thus, as the dimmer switch is manually adjusted, the value of R1 changes, thereby changing the off-time, (often referred to as the phase delay). As R1 is increased, less power goes to incandescent bulb and brightness is reduced. Shown below are a typical phase dimmer installed, and its simplified electronics schematic.

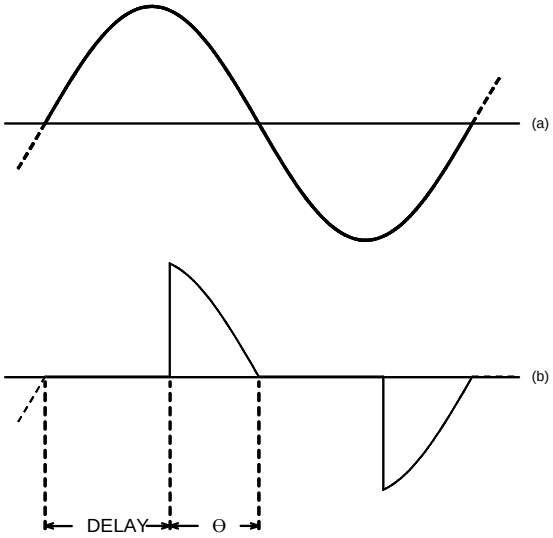


Adjusting the light level with a traditional dimmer only requires the sliding or turning of the front panel slider/knob. This adjustment increases or decreases the resistance of resistor RI shown in the schematic. By changing the value of this resistor the amount of current allowed to charge capacitor C1 increases and decreases, and controls the turn on of the Triac/Diac pair within the dimmer. Simply put, by changing the resistor value, you change the incoming AC conduction angle (firing angle).

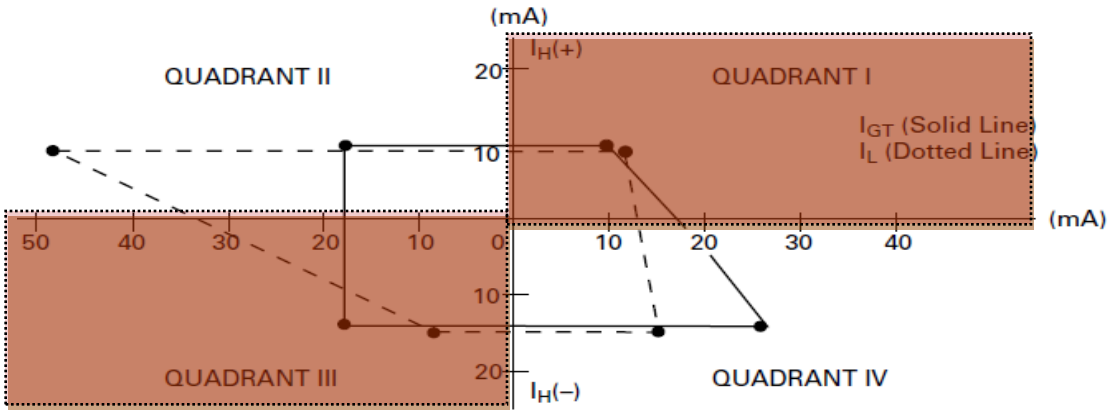
There are two basic types of phase dimmers on the market, forward phase dimmers, and reverse phase dimmers.

Forward Phase Dimmers (aka leading edge dimmers)

Forward phase dimmers are all dimmers where the fast rising edge of the AC waveform goes from 0 volts to some positive or negative voltage. Forward phase dimmers control the amount (average) voltage seen by an incandescent bulb by turning on once enough current charges up capacitor C1 and turns on the Triac within the dimmer.



All forward phase dimmers operate in the first and third quadrant, i.e. the triac as a switch will have its current and voltage across the device positive, or its voltage and current across the switch negative only. This is illustrated in the below graph.



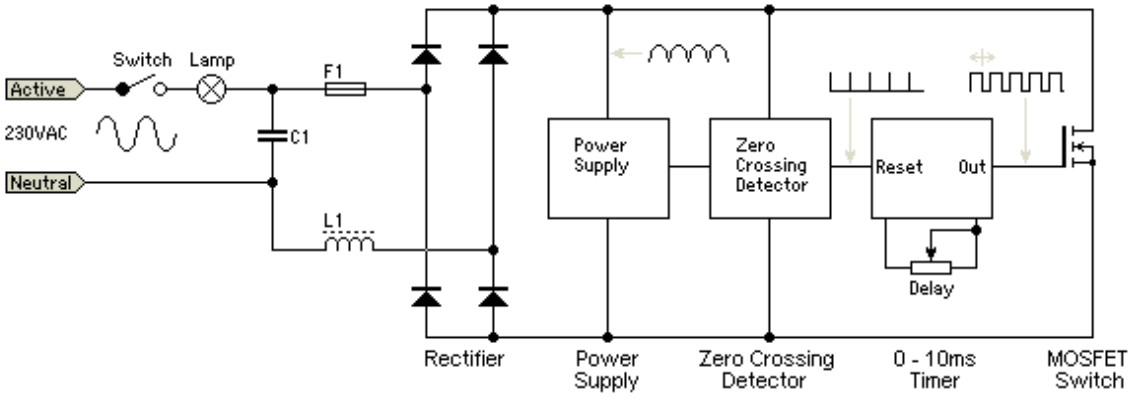
- IGT = “Gating current” or firing current
- ILT = “Latching current” or holding current

From the graph above, the holding and firing currents are different in quadrant one and three. This will manifest itself as a technical challenge for SSL solutions, which will be discussed later in this document.

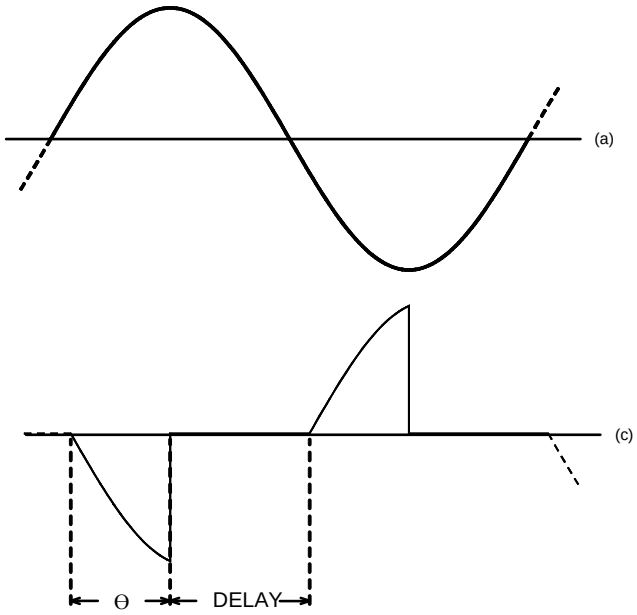
Reverse Phase Dimmers (aka trailing edge dimmers)

Reverse phase dimmers are less common than forward phase dimmers, but are common. Reverse phase dimmers are used instead of forward phase dimmers with Halogen low voltage systems (including electronic low voltage transformers), systems where RFI is an issue. Reverse phase dimmers, or also known as trailing edge dimmers are more expensive due to the electronics found internal to the dimmer.

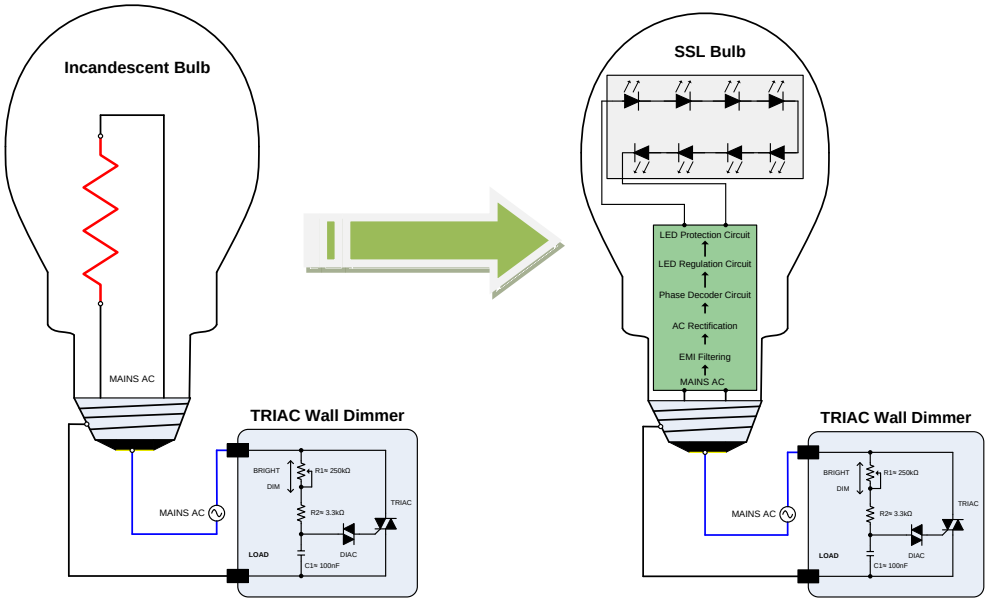
Reverse phase dimmers are electrically constructed differently than forward phase dimmers. Instead of Diac/Triac pair, reverse phase dimmers use MosFET/IGBT pair, zero cross detection and delay circuitry to define the conduction angle of the AC waveform.



Reverse phase dimmer AC waveform with and without dimmer inline shown below.



SSL/tradition phase dimmers compatibility issues



The SSL fixture/bulb and its compatibility with a traditional phase dimmer presents numerous technical challenges to produce a well operating, reliable cost effective system.

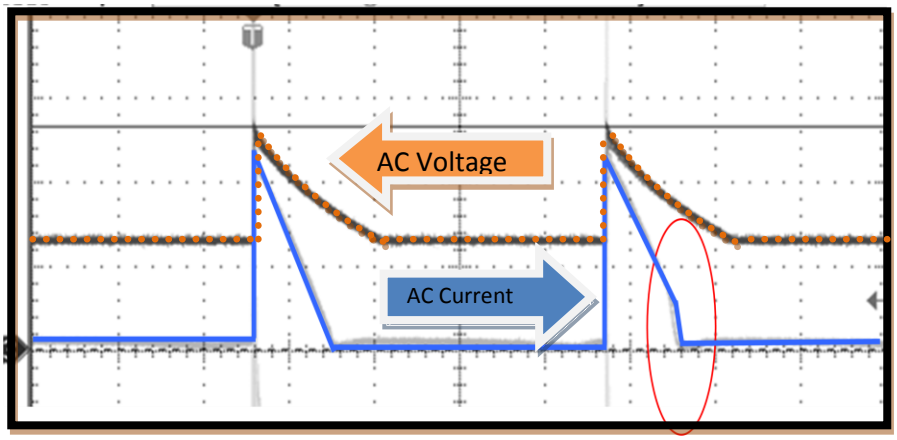
An incandescent light source can be modeled as a power resistor with only 4% of the power consumed resulting in visible light. On the other hand, SSL solutions have about 40% to 50% of the power consumed converted into visible light, but require dozens of integrated circuits (IC's), resistors, capacitors, and inductors to operate properly. This complexity added with regulatory standards such as UL/CSA, FCC, and Energy-Star, turns a simple task of producing light into a complex engineering accomplishment.

Forward Phase Dimmers & SSL Compatibility Issues

Summary issue #1 – Loss of holding current

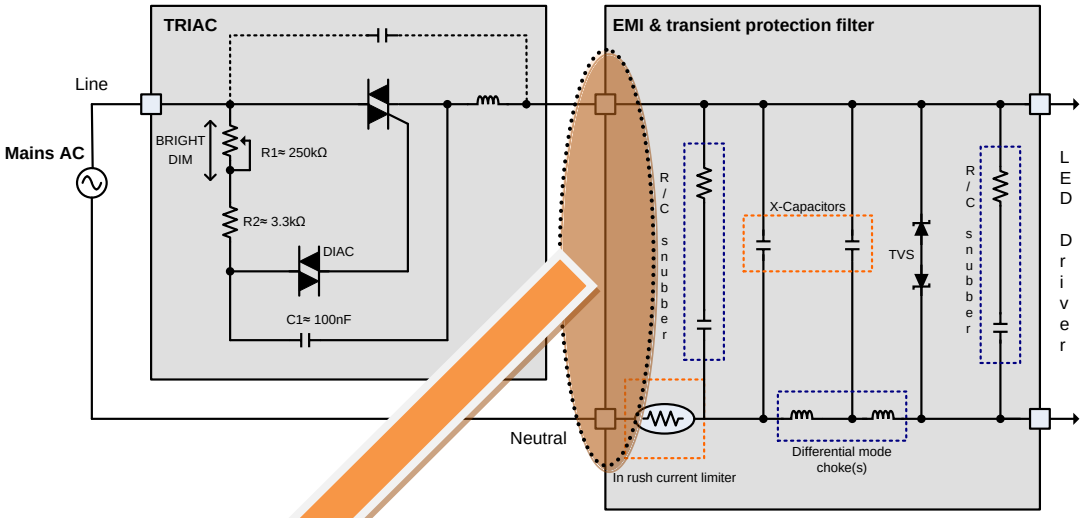
Forward phase dimmers typically use triac's. In order for a triac to work properly, it must have a minimum holding current through it. Incandescent light bulbs act as a resistor, and are so inefficient that an inadequate amount of holding current has never been an issue. LEDs are so efficient that they sometimes aren't using enough line current, especially at low dimming, that the triac will "miss-fire" during normal operation. Additional line current must be drawn when dimming at low conduction angles.

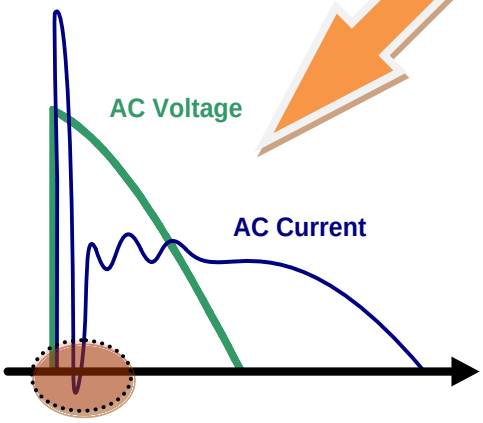
The scope capture below illustrates an actual SSL bulb losing its holding current during low conduction angles. The second (blue) waveform shows a sudden drop-off of AC current. This is loss of holding current is often seen initially on every other AC cycle. This is due to the non-symmetry of the triac operating in quadrant I/III.



This loss of holding current in one quadrant will be noticed as 60Hz (N. America) flutter depending on IC used, decode method etc.

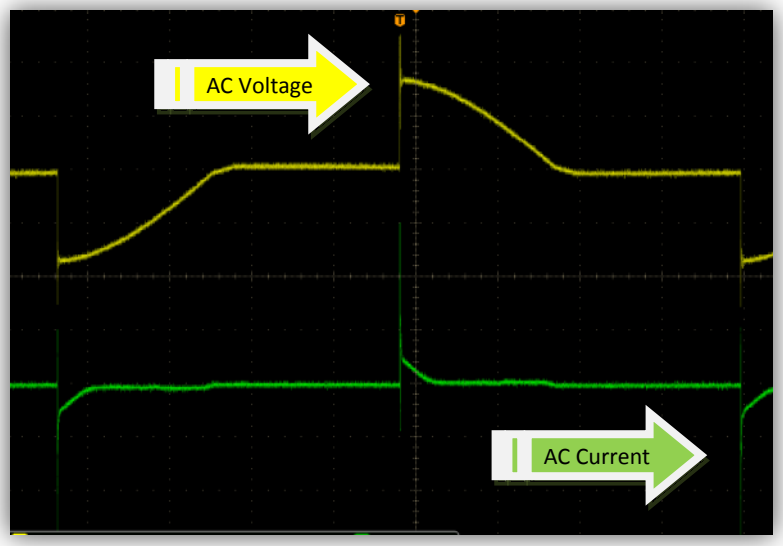
Summary issue #2 – EMI plus fast rising edge of forward phase dimmer turn off (ringing)



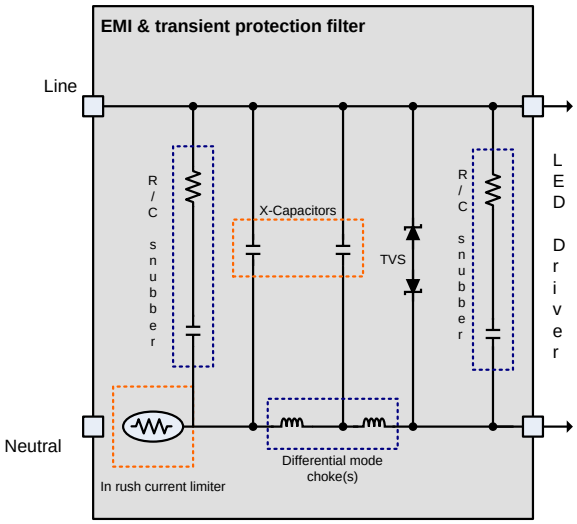


The combination of a fast voltage edge with reactive components within the EMI filter inflicts an AC current ring that can be severe enough to ring negative. One the ring reaches zero, or negative the Triac will turn off. It is imperative the final product be tested with phase dimmers with an EMI filter that ensures FCC/EMI compliance. Testing w/o EMI filter offers no valuable information.

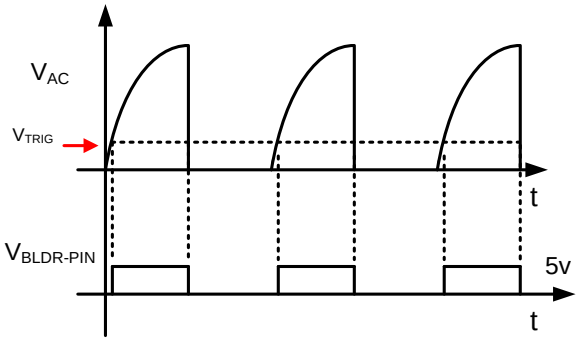
Actual Phase Dimmer in-line with AC current ringing negative capture

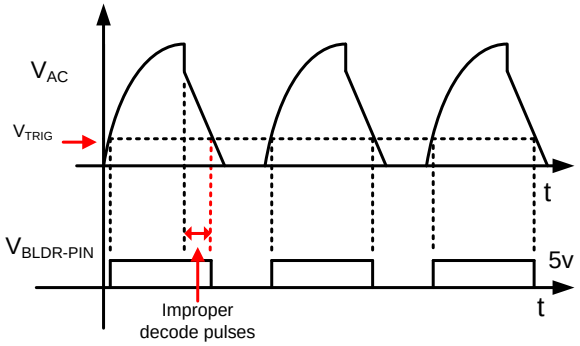

AC Voltage
AC Current

Reverse Phase Dimmers & SSL Compatibility Issues



Reverse phase dimmers **do not** suffer from a minimum amount of holding current required as the forward phase dimmers. Reverse phase dimmers are straightforward to make compatible with SSL fixtures compared to forward phase dimmers. Higher efficiency, less noise due to falling voltage transition is a few attributes of reverse phase dimmers. However reverse phase dimmers can create design challenges when paired with SSL fixtures. Depending on how the electronics within the SSL system decodes the phase dimming conduction angle a problem arises when the phase dimmer turns off, but enough parasitic capacitance within the EMI filter and power conversion circuit bleed the voltage off of the line slowly. This confuses some decode circuits, and steps must be made to remove the charge from the circuitry quickly.





The illustrations above shows the rectified AC line voltage from a reverse phase dimmer. The lower square wave waveforms are decode representations of the AC line voltage. The right-hand illustration shows improper decode due to the slow bleed off of the AC line waveform.

NSC/TI Phase Dimming Solutions

LM3445 & LM3448 SSL driver with phase decode circuitry

The LM3445 was released from National Semiconductor in 2008, and the LM3448 is being released in September of 2009. The LM3445 was the industries first SSL with phase dimming decode circuitry. The LM3448 has the same control architecture as the LM3445, and contains an integrated 600V switching MosFET.

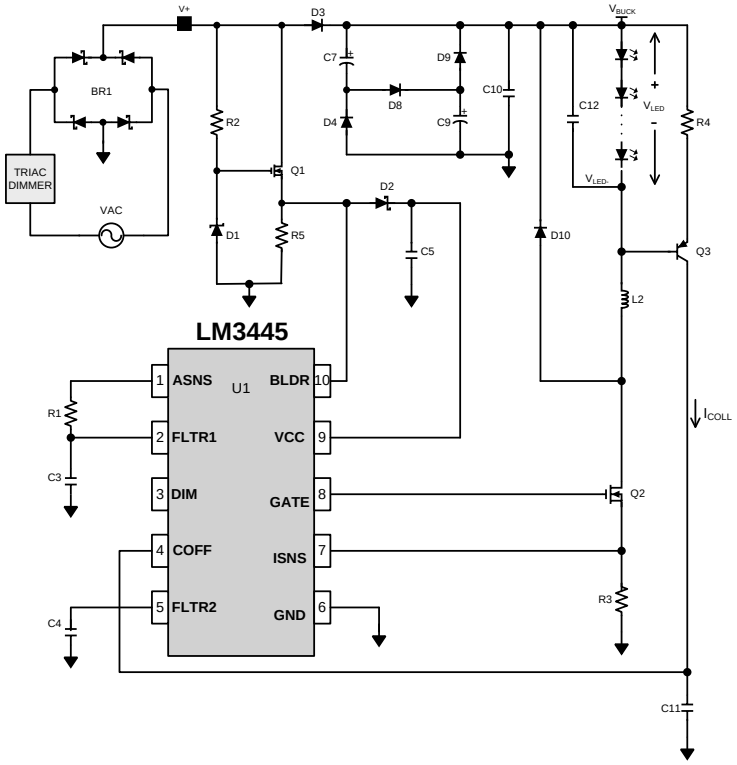
Currently there are numerous application notes and a datasheet that outlines the operation of the LM3445/48 on our website. This section of the phase dimming workbook is intended to supplement these documents. Please refer to the data sheet(s) and application notes for detail IC "Theory of Operation".

The LM3445 and LM3448 is a versatile IC that can be used configured in the following topologies:

- AC/I_{LED} Non-isolated Buck Topology
- AC/I_{LED} Non-isolated Buck Topology with line injection
- AC/I_{LED} Non-isolated Buck/Boost Topology with line injection
- AC/I_{LED} Isolated Flyback Topology with primary power regulation

LM3445/48 AC/I_{LED} Non-isolated Buck Topology

Simplified LM3445 Buck Topology with phase dimming decode

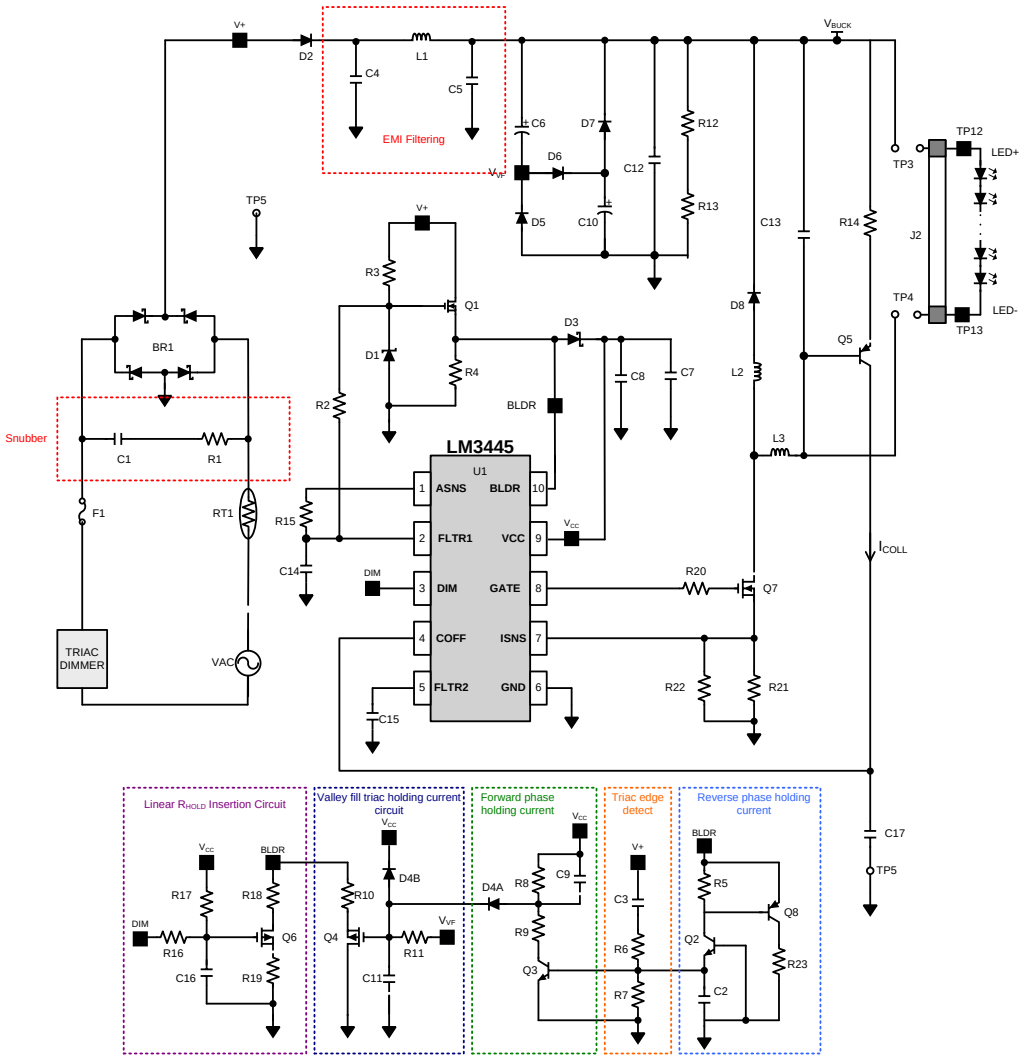


This circuit works well with both forward and reverse phase dimmers, but draws power (holding current) from the input through the entire cycle. This is accomplished by resistor R5. The lower the resistance, the more current pulled from the AC line (phase dimmer).

An optimal method is to apply just enough holding current at the right time in the cycle to keep the triac operating properly. This will ensure no variation or 'flicker' is seen in the LED light output and will improve the circuit efficiency. We will examine circuits that do this for both forward and reverse phase triac dimmers.

LM3445 Non-Isolated Non-Dimmable LED Driver Demonstration Board

- **Strengths**
  - Low Cost
  - LED current = DC (no 120Hz)
  - Small solution size
  - Great dimming ratio (100:1)
  - Great efficiency when optimized (eff > 85%)
- **Weakness**
  - Not isolated
  - Heavy component count



Practical LM3445 Buck Topology with phase dimming decode and forward & reverse phase dimmer compatibility circuits

The circuits shown in the bottom of the schematic are designed to identify the type of phase dimmer in-line with the LM3445, and add holding current, or current to discharge parasitic capacitances. The objective is to only add enough holding current as needed. This allows the manufacture to optimize efficiency and gain Energy Star approval if desired. The following sections give details on the operation of these circuits.

When to add triac holding current

Depending on the triac used internal to the dimmer, a large amount of holding current maybe required (I_{HOLD} > 25mA). If an ELV (reverse phase dimmer) is used only a small amount of holding current may be required (I_{HOLD}< 2mA).

In short, if you know what type of dimmer is being used a LED driver solution (LM3445/48) circuit can be optimized. If you would like the LM3445/48 to work with all dimmers, you will need to design for worst case scenarios.

The following graphs and illustrations below demonstrate methods to assure proper phase-dimmer/SSL solution compatibility. One could simple place holding current throughout the whole AC cycle by means of resistor (R4), or place just enough holding current at the proper time during an AC cycle. The simplest form of Triac holding current is to place a resistor (R4) from the source of Q1 (Bleeder pin of the LM3445) to ground. This pulls current from the input during the full half cycle of the rectified AC waveform regardless if it is required.

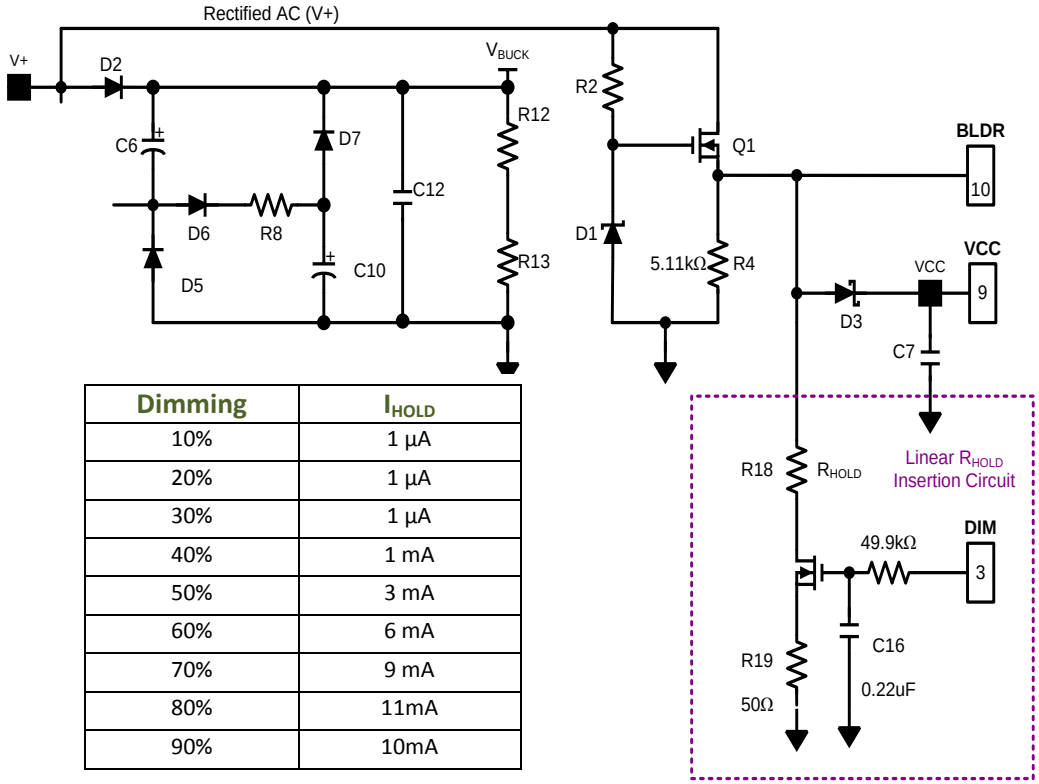
Phase Dimming Circuits Analyzed

NSC/TI has developed some unique phase dimming circuits that place holding current only when needed

- Low Dimming Linear Hold
- Valley Fill Hold
- Forward phase hold
- Reverse phase hold

Linear R_{HOLD} circuit SM EVB non-isolated PCB

The LM3445 has pin labeled “DIM”. This pin outputs a PWM signal that is inversely proportional to the conduction angle of the AC line voltage. As an example if the phase dimmer had a large conduction angle 135° the PWM output would be 10% to 20%. If the conduction angle was low (25° - 45°) the PWM signal would be large 70% to 80%. This information allows the user to create a circuit to add holding current only during low conduction angles. A circuit we developed is shown below. The PWM signal is filtered to a DC level and a P-Channel FET adds holding current as the gate-source voltage changes.

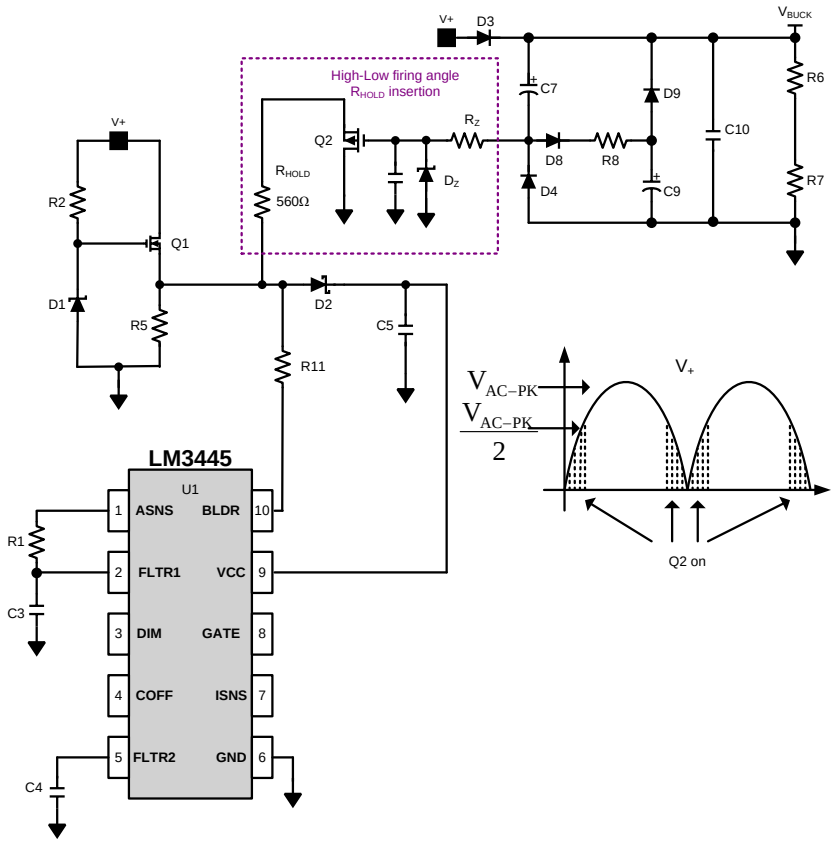


Dimming	I_{HOLD}
10%	1 µA
20%	1 µA
30%	1 µA
40%	1 mA
50%	3 mA
60%	6 mA
70%	9 mA
80%	11mA
90%	10mA

LM3445/48 non-isolated triac holding current Valley Fill circuit

The non-isolated LM3445 Buck Topology circuit described uses a simple “Valley-Fill” circuit so that a power-factor of 0.90 is achieved. The valley-fill capacitors C7 & C9 are charged in series until the line voltage decreases to ½ of its peak value. Once this occurs capacitors C7 & C9 are in parallel. When the capacitors are in series power (current) is being pulled from the AC line and any minimum holding current requirements are satisfied. When the capacitors are in parallel, there is a brief period of time where the output load is being supplied by these two capacitors. Therefore there is minimal or no line current being drawn from the AC line and the minimum holding current requirement is not met. The triac may turn off at this time, which causes phase dimming decode issues.

A simple circuit is used to add holding current when valley fill diode D4 is conducting



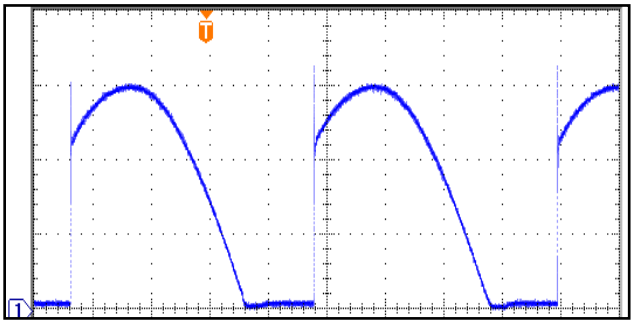
Detecting a Triac Dimmer, and Reverse Phase and Forward Phase Detection

During initial turn on (forward phase) or turn off (reverse phase) of a phase dimmer a little extra holding current is sometimes required to latch the phase dimmer on, or discharge any parasitic capacitances on the AC line.

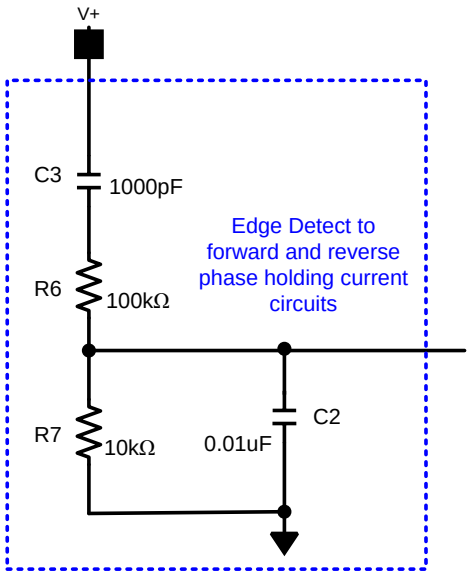
Knowing that the triac requires its holding current during the last portion of the AC cycle, and that with a reverse phase dimmer there is a sharp voltage transition from high to low allows the below circuit to be used for reverse phase dimmers.

Triac Detect

The waveform to the right is an example of a forward phase triac dimmed rectified AC (V+) voltage. C3 and R6 are sized to respond to this edge and are used create a positive voltage at the base of Q3 (see forward phase circuit). The value of R7 can be adjusted to vary the sensitivity of the edge detect circuit. The beauty of this circuit is that if a triac is NOT present, the circuits will not turn on, and therefore the circuit is very efficient. This is important when trying to achieve Energy Star compliance. When testing ids performed for Energy Star, no triac is present.

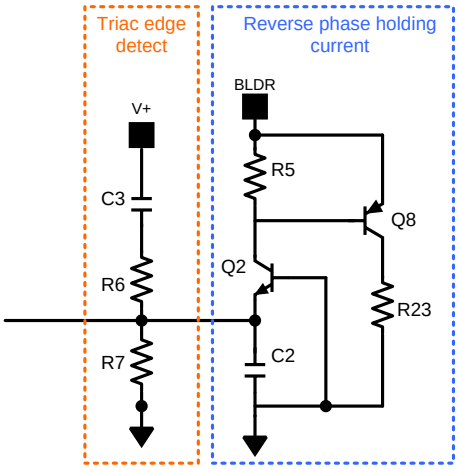


LM3445 reverse & forward phase edge detect circuit



LM3445 edge detect + reverse phase holding current circuits

The series connected resistors and capacitor from the rectified AC line will detect the high -dv/dt transition and bias the transistor, applying R_{HOLD} (R5) resistor.

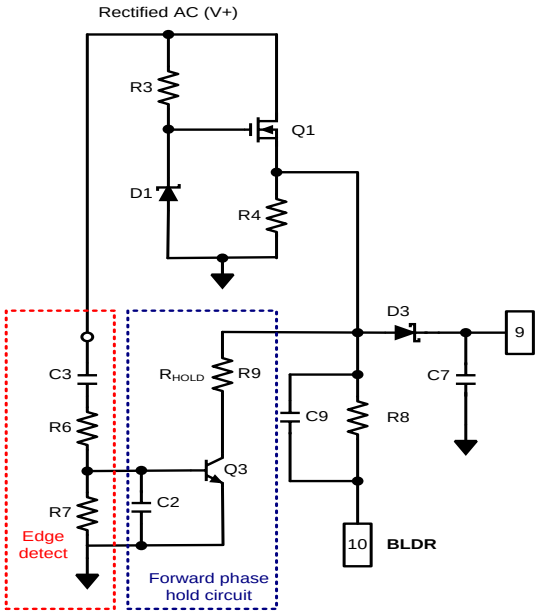


LM3445 edge detect + forward phase holding current circuits

The forward phase triac dimmer (which is more common) still requires the holding current at the last portion of the AC cycle. The fast transition, or high +dv/dt happens earlier in the cycle although. Remember, it is the last few degrees of the AC cycle where the triac holding current needs to be applied, not the first portion of the AC cycle.

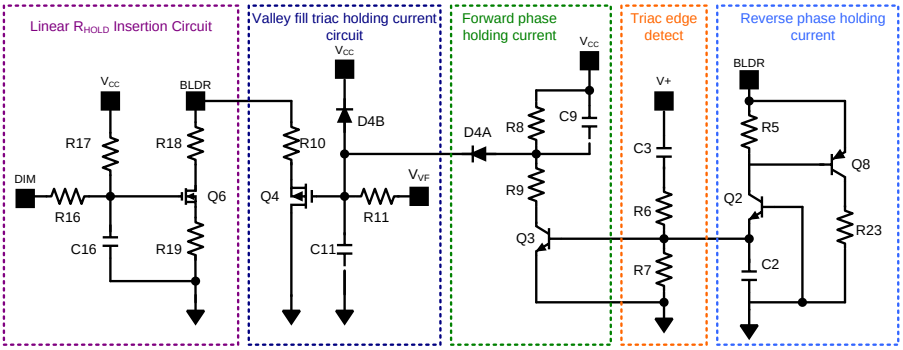
The circuit shown below applies the holding current of the first and last portion of the AC cycle. By using the same edge detection circuit as the reverse phase dimmer, we can add circuitry to disable the circuit when no high dv/dt is detected (not present).

Therefore a combination of circuit #1 and circuit #2 disables the R_{HOLD} resistor when the triac/phase dimmer isn't present, and applies the R_{HOLD} resistor only when desirable. This circuit works with reverse and forward phase dimmers, and is illustrated below:

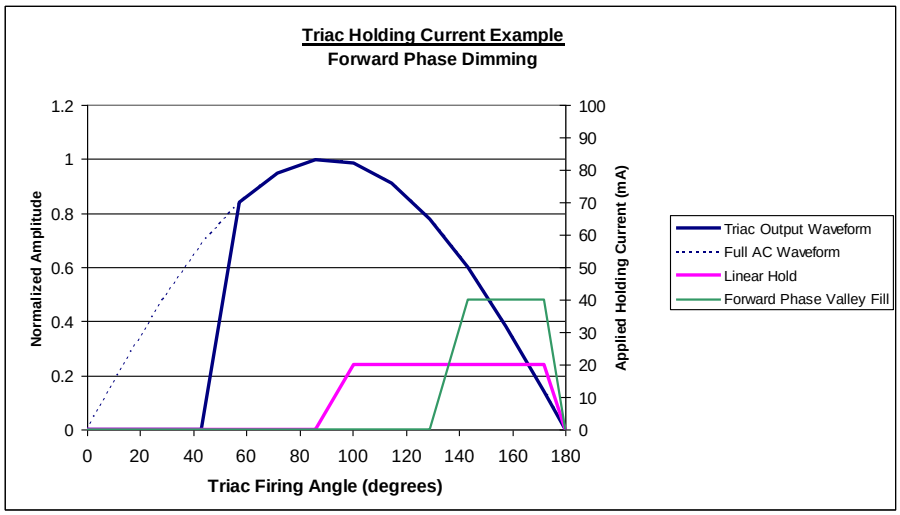


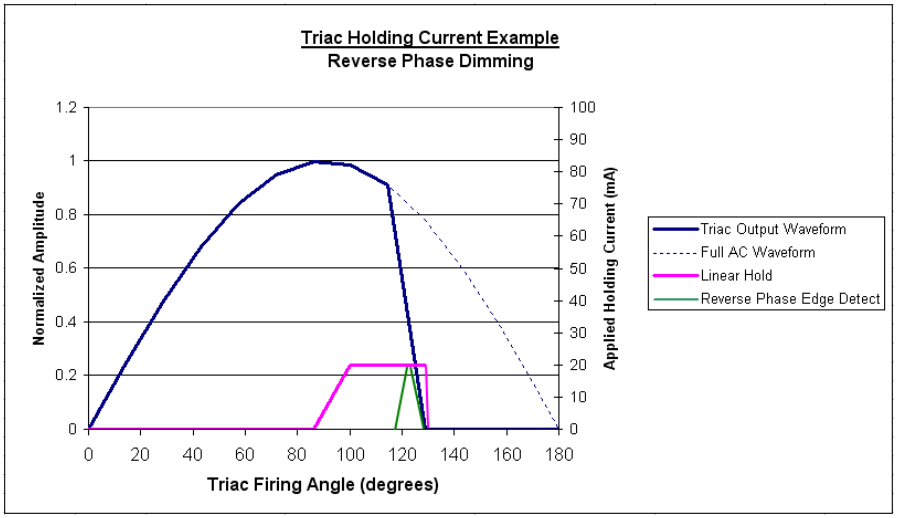
LM3445 Valley-Fill Evaluation PCB External Circuit Performance Summary

Close up of external circuitry to improve efficiency

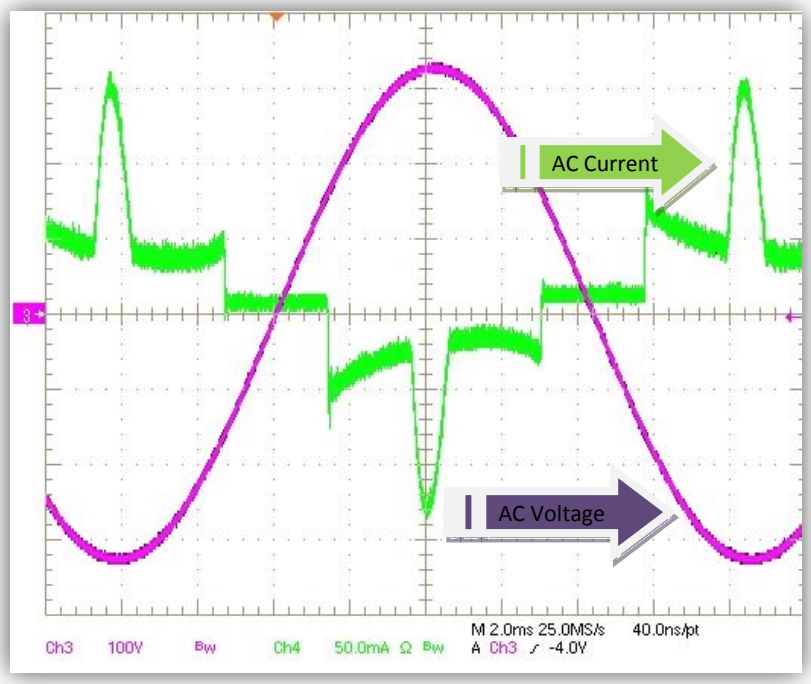


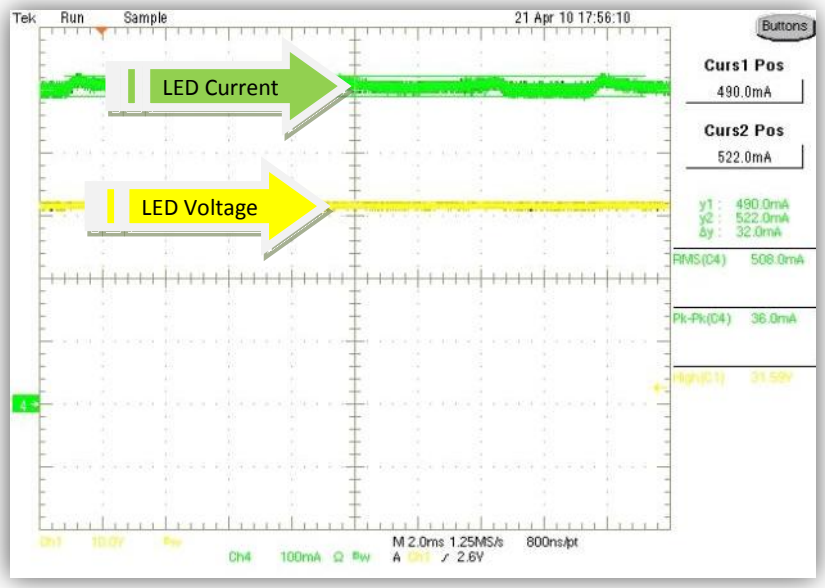
The following charts illustrate the combined loading and timing of each circuit for a sample triac firing angle.





LM3445 AC/I_{LED} Non-isolated Valley-Fill Buck Topology Waveforms





LM3445/48 Constant Frequency DCM Flyback (Isolated) Topology Designs

LM3445 Summary of Trade-offs

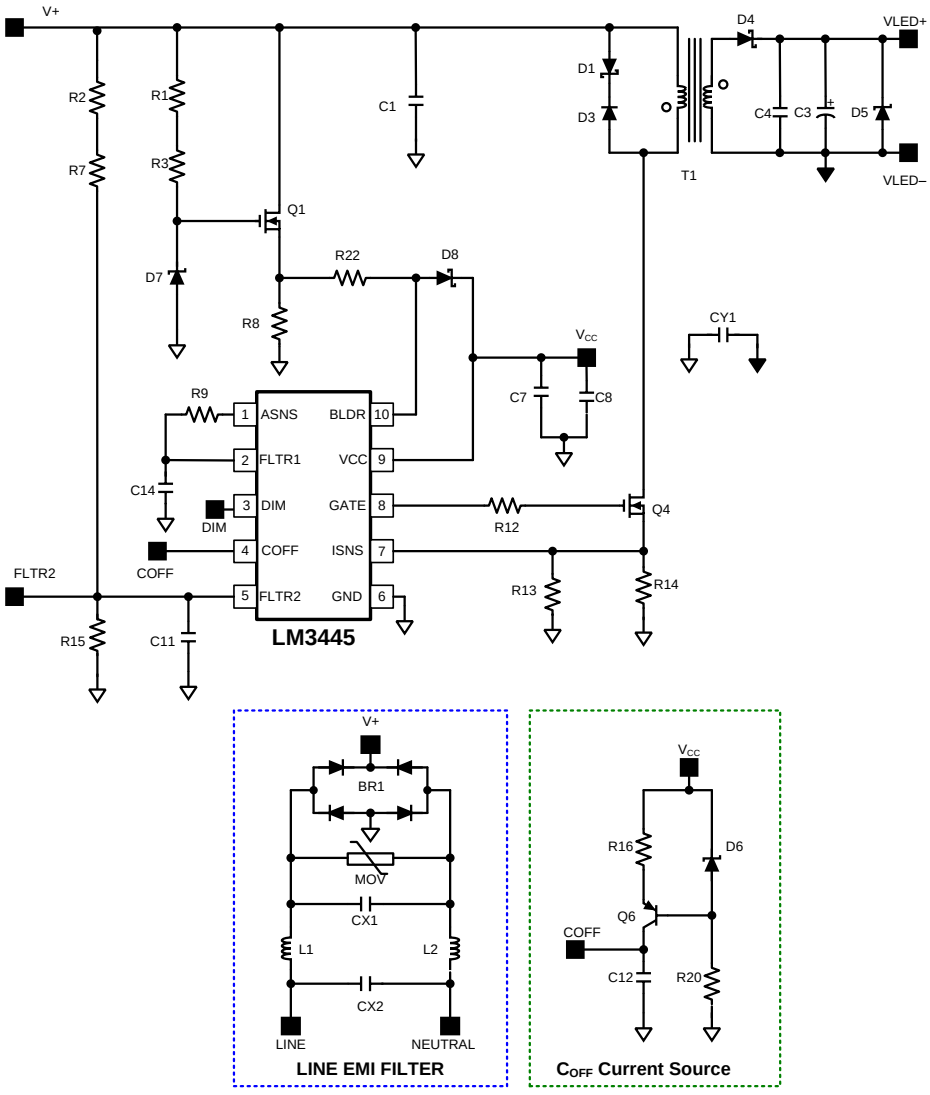
Strengths

- Dimming capable (Dimm ratio ~ 40:1)
- Isolated
- Power Factor > 0.95

Weakness

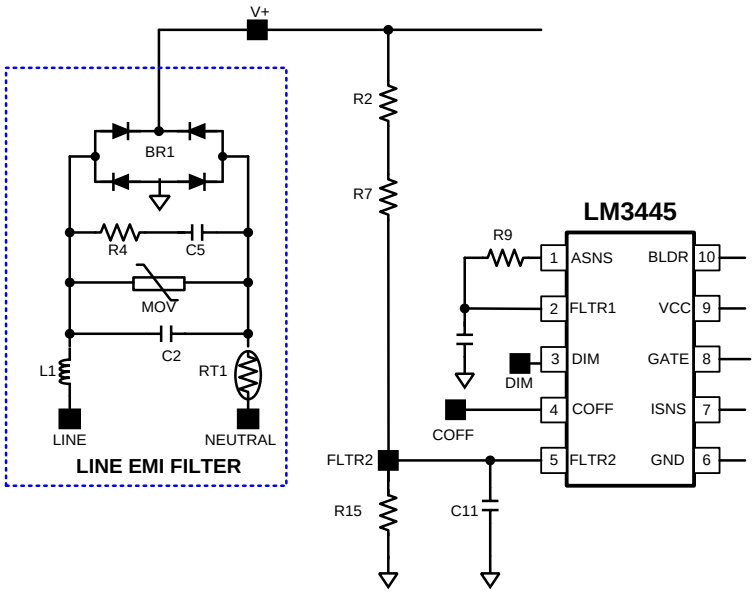
- Medium cost (transformer)
- 120Hz ripple in LEDs (magnitude depends on capacitor size)

LM3445 Isolated Flyback Typical Schematic

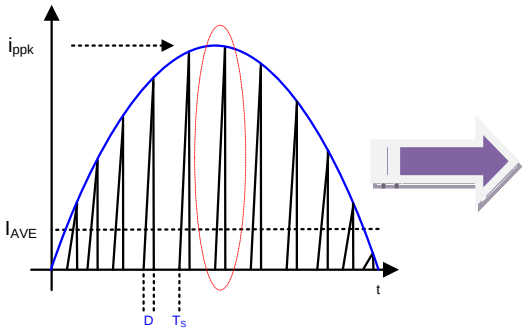


Injecting line voltage into Filter-2 pin (achieving PFC > 0.95)

If a small portion (750mV to 1.00V) of line voltage is injected at FLTR2 of the LM3445/48 (internal reference), you essentially turn the LM3445/48 circuit into a constant primary power flyback. The LM3445/48 works as a constant off-time controller by injecting the 1.0V rectified AC voltage into the FLTR2 pin, the on-time can be made to be constant, and therefore a constant switching frequency DCM Flyback converter is created.

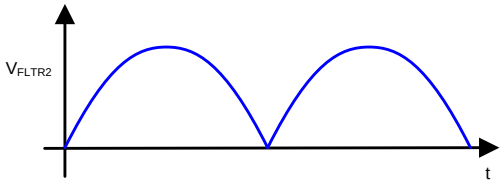


With a DCM Flyback, Δi needs to increase as the input voltage line increases. Therefore we could ideally have a constant on-time (inductor L is constant).



$$V_{IN} = L\frac{di}{dt} \quad \& \quad \frac{L}{t_{ON}} = \frac{V_{IN}}{\Delta i}$$

FLTR2 pin has the following wave shape on it with no triac dimmer in-line



Voltage at VFLTR2 peak should be kept below 1.00V. At 1.25V current limit is tripped. C11 is small enough not to distort the AC signal, but add a little filtering.

LM3445 Isolated FLTR2 120VAC typical design

- R2 = R7 = 124kΩ
- R15 = 1.50kΩ

Therefore:

- V_{IN} = 135VAC VFLTR2 = 1.14V
- V_{IN} = 90VAC VFLTR2 = 0.779V

LM3445 Isolated FLTR2 220VAC typical design

- R2 = R7 = 309kΩ
- R15 = 1.74kΩ

Therefore:

- V_{IN} = 260VAC VFLTR2 = 1.03V
- V_{IN} = 180VAC VFLTR2 = 0.714V

LM3445/48 Flyback Duty Cycle Calculation

$$D = \frac{\left(V_O \times \frac{N_P}{N_S}\right)}{\left(V_O \times \frac{N_P}{N_S}\right) + \left(V_{IN}\right)}$$

Maximum Duty Cycle

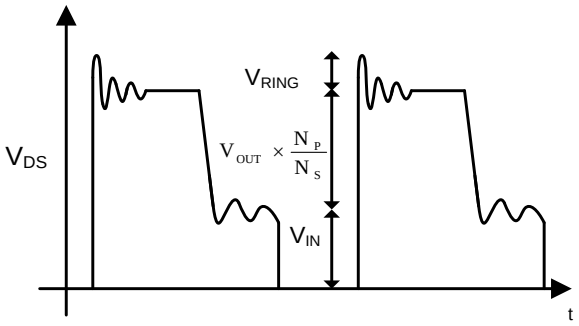
$$D = \frac{\left(V_O \times \frac{N_P}{N_S}\right)}{\left(V_O \times \frac{N_P}{N_S}\right) + \left(V_{IN\text{-}MIN}\right)}$$

LM3445 Flyback MOSFET Selection

The maximum Drain to Source voltage (V_{DS}) of the main switching FET is defined within the device datasheet. The maximum operating drain to source voltage is calculated in the following manner.

Often a design engineer will know what /MOSFET he would like to use in a design. If this is the case then the maximum turn's ratio can be calculated at this point.

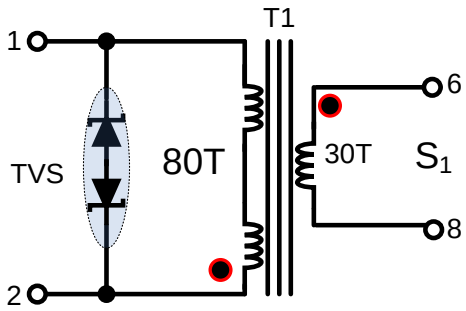
$$V_{DS-MAX} = V_{RING} + V_{IN} + V_{OUT}\left(\frac{N_P}{N_S}\right)$$



- V_{RING} depends on the design of the transformer, and more specifically the leakage current. I usually design for 50V of ringing, and often I design with 100V of ringing for margin.
- The maximum input voltage (V_{IN}) equals the maximum input AC voltage times 1.414
- V_O is equal to the highest output voltage expected.
- Assume we want a 600V MOSFET
- Therefore NP/NS maximum would be 5:1. I will choose 4:1 for margin

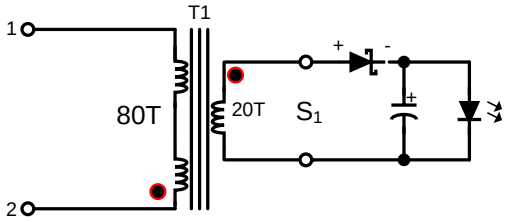
Due to a transformer's inherent leakage inductance, some ringing VRING on the drain of the SW FET will be present and must also be taken into consideration when choosing a turns ratio. V_{RING} will depend on the design of the transformer. A good starting point is to design for 50V of ringing while planning for 100V of ringing if additional margin is needed. The maximum SW FET drain-to-source voltage is calculated based on the specified output voltage V_O, ringing on the SW FET drain and the maximum peak input voltage V_{IN}-PK(MAX),

TVS selection



TVS breakdown voltage should be greater than the output voltage x turns ratio. If LED stack voltage equals 25V, and you have a 4:1 turns ratio, TVS > 100V

Output Diode



$$V_D = V_O + \frac{V_{INMAX}}{n_{PRI}/n_{SEC}}$$

Example:

- V_{IN} = 135VAC
- V_O = 36V
- n_{PRI} = 80T
- n_{SEC} = 20T

V_{RR} > 85V

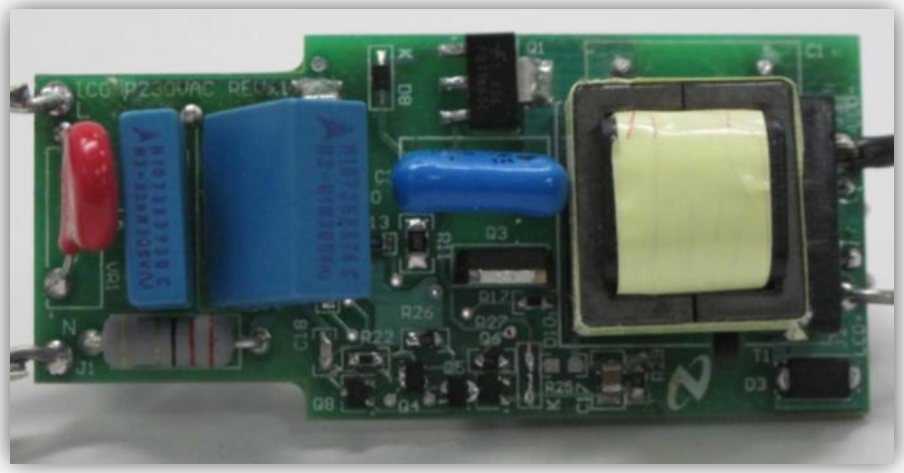
LM3445/48 Flyback Topology Typical Design Example

LM3445 - 120VAC, 15W Isolated Flyback Driver

The LED driver board is designed using LM3445 to generate an output power of 15W suitable for powering an LED stack with forward voltage drop of 36V and forward current of 350mA.

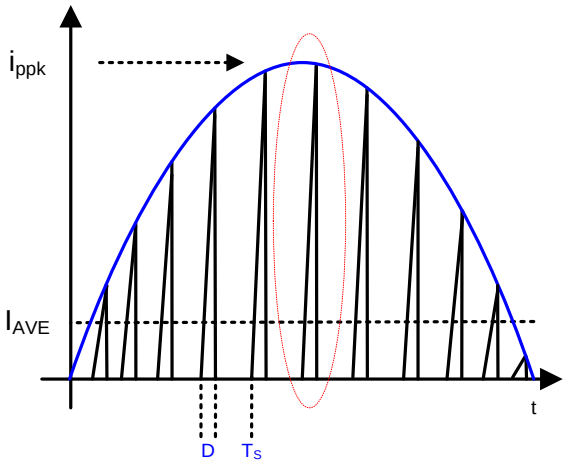
Symbol	PARAMETER	Min	Typ	Max
V_{IN}	Input voltage	95 Vrms	120 Vrms	135 Vrms
V_O	LED string voltage	35 V	36 V	38 V
I_{LED}	LED string average current	-	350 mA	-
P_O	Output power	12.5 W		
fsw	Switching frequency	-	75 kHz	-

LM3445 Typical Flyback Solution



Transformer Design

Peak Input Current Calculation



$$I_{IN-AVE} = \frac{P_{OUT}}{\eta \times V_{DC-MIN}} = 115mA$$

$$Energy = \frac{1}{2} \times L \times i_{ppk}^2$$

$$i_{PPK} = \sqrt{\frac{P_{OUT} \times 2}{f_{SW} \times L}}$$

Area of the triangle = 1/2 base x height

$$i_{PPK} = \frac{2 \times I_{AVE}}{D} \approx 500mA$$

Primary Inductance Calculation

Need to keep converter in DCM. Worst-case scenario is when converter is operating a minimum input line voltage (90VAC). Calculate primary inductance at this point, and reduce inductance for tolerance, and margin.

$$V = L \frac{di}{dt}$$

$$L = \frac{V_{IN-MIN} \times D_{MAX}}{f_{SW-MIN} \times i_{PPK}} \approx 1.5mH$$

Guarantee DCM therefore 1.2mH target

Calculating Primary Turns

Maximum operating flux density for most cores is 0.2T

$$B_{MAX} = \frac{L_{PRI} \times i_{PPK}}{N_{PRI} \times A_e}$$

Where Ae equals the specific cores effective area.

- EFD20 effective core parameters (example) = 31mm2
- EE16 effective core parameters (example) = 19mm2

$$N_P = \frac{L_{PRI} \times i_{PPK}}{B_{MAX} \times A_e}$$

B = Tesla - L = Henrys - Ae = m^2

$$N_P = \frac{1200 \times 10^{-6}(0.5A)}{(0.25T) \times 19 \times 10^{-6} m^2} \approx 124 \text{ Turns}$$

Alternatively:

$$N_P^2 = \frac{L_{PRI}}{A_L}$$

Choose an AL, and calculate primary turns. Graphs similar to the one on the right are quick and simple to use. Define AL (100nH/T2), and then determine gap. Look for standard AL numbers when designing your transformer.

$$N_P = \sqrt{\frac{L_{PRI}}{A_L}} \approx 110 \text{ Turns}$$

- WB - Bobbin width is equal to dimension 13mm from the above illustration.
- WM - Equals the margin tape required width.
- OD – Outside diameter of the wire used.

As an example, if we have 18mm of bobbin width, and we want to add 4mm of tape on each side, then we have 10mm of width.

I want to split the primary into two windings (series connected), 80T total, 40T across bobbin. There are only four pins per side of the EFD20 bobbin we want to use. Therefore, the primary is split, and a flying lead is necessary. What is the maximum wire width I can use?

$$O_{D\text{-}MAX} = \frac{W_B - 2W_M}{\text{Turns}} = 0.32\text{mm}$$

- 28-gauge wire has an OD of 0.321mm diameter
- 30-gauge wire has an OD of 0.255mm diameter
- 32-gauge wire has an OD 0.202mm diameter
- 34ga wire has an OD of 0.160mm diameter
- 36-gauge wire has an OD 0.127mm diameter

Gauge to diameter and vice versa conversion

http://www.66pacific.com/calculators/wire_calc.aspx

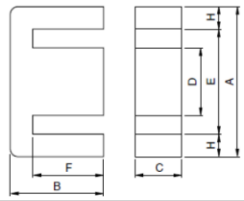
Triple insulated wire

http://www.furukawa.co.jp/makisen/eng/product/texe_series.htm

We need to guarantee that the primary inductance keeps us in DCM. Therefore reduce turns to 80T

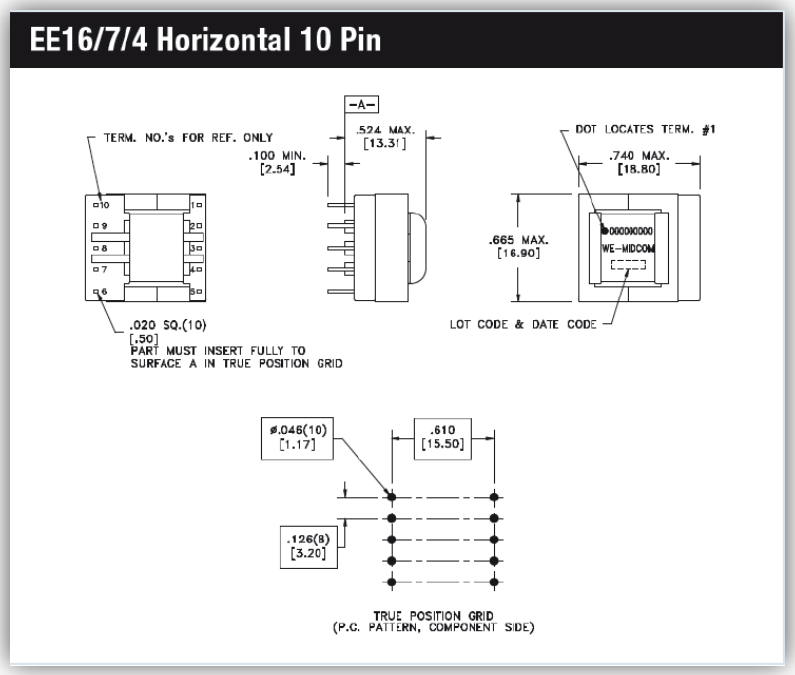
LM3445 Flyback Design Example

E16/7/4



Part No.	JIS	Dimensions in mm inches A	B	C	D	E min.	F	H	I
PC40EE16-Z	JIS FEE 16A	1	16.0±0.3 .630±.012	7.15±0.15 .281±.006	4.8±0.2 .189±.008	4.0±0.2 .157±.008	11.7 .461	5.1±0.2 .201±.008	2.0 .079

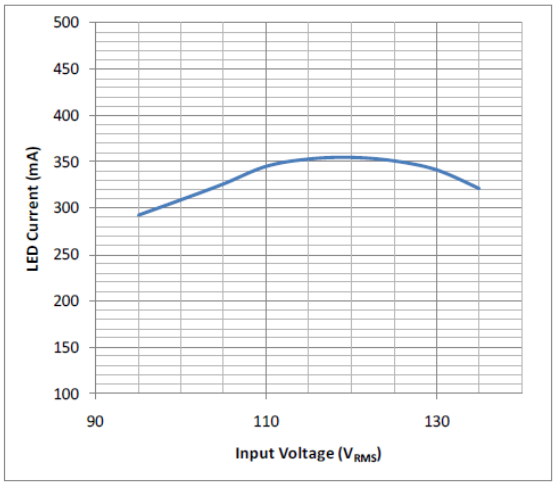
Part No.	Effective parameter C1 (mm⁻¹)	Ae (mm²)	ℓe (mm)	Ve (mm³)	Electrical characteristics AL-value (nH/N²)* Without air gap	With air gap	Core loss (W) max. 100kHz, 200mT, 100°C	Wt (g)	Bobbin item
PC40EE16-Z	1.82	19.0	34.5	656	1140±25%	80±7% 160±10%	0.31	3.3	BE16-116CPFR BE16-118CPHFR BE16-1110CPNFR



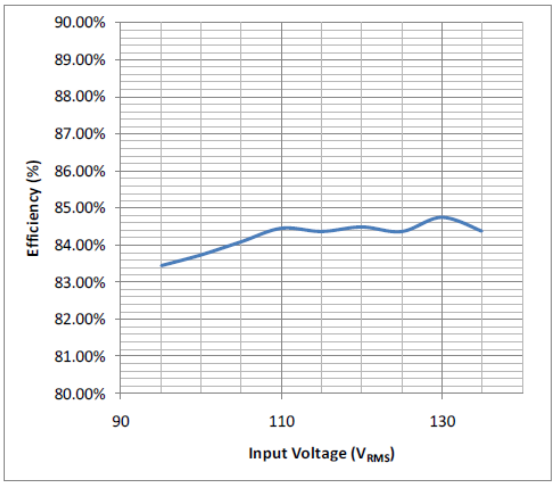
Parameter	Value
AL	85.4 nH
Primary turns	120
Secondary turns	24
Auxiliary turns	11
Primary inductance	1.23 mH
Secondary inductance	49.2 µH
Auxiliary inductance	10.3 µH

Empirical Results/Performance

Input Voltage (Vrms)	Input Current (mArms)	Power Factor	Input Power (W)	Output Voltage (V)	Output Current (mA)	Output Power (W)	Efficiency (%)
95	133.8	0.991	12.58	35.84	292.9	10.49	83.45%
100	134.6	0.99	13.29	35.98	309.3	11.12	83.74%
105	135.1	0.989	14.02	36.13	326.3	11.78	84.09%
110	136.5	0.989	14.83	36.3	345	12.52	84.45%
115	134.1	0.986	15.21	36.37	352.8	12.83	84.36%
120	129.3	0.985	15.27	36.39	354.5	12.90	84.48%
125	123.2	0.981	15.12	36.36	350.8	12.75	84.36%
130	115.1	0.975	14.6	36.26	341.2	12.37	84.74%
135	106.1	0.966	13.74	36.08	321.3	11.59	84.37%



Line regulation



Efficiency

Current Limit

The peak current limit I_{LIM} should be at least 25% higher than the maximum peak input current under worst case operating conditions.

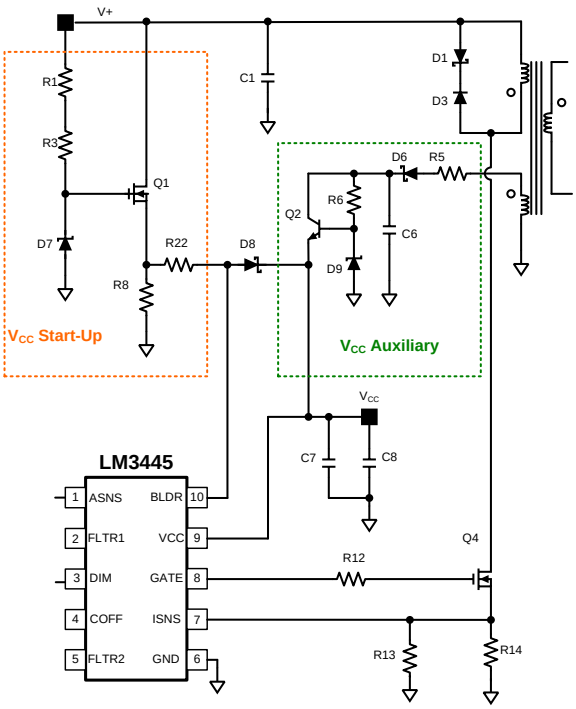
$$1.27V = I_{LIM} \times \left(\frac{R13 \times R14}{R13 + R14} \right)$$

With 25% margin

$$\left(\frac{R13 \times R14}{R13 + R14} \right) = \frac{1.27V}{1.25 \times I_{LIM}}$$

BIAS SUPPLIES

The primary bias supply circuit consisting of Q1, R1, R2, D7 enables instant turn-on. The auxiliary supply provides bias during normal operation allowing for high efficiency in steady state operation.



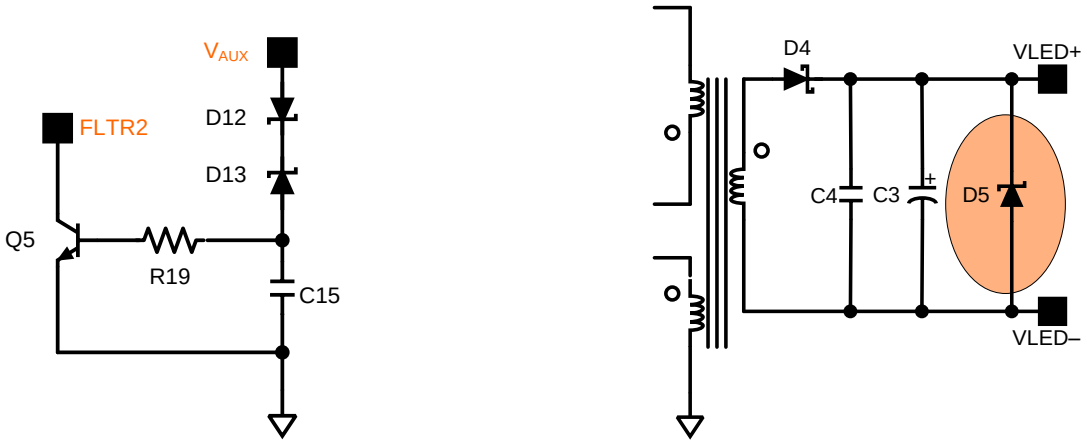
The passFET (Q1) is used in its linear region to stand-off the line voltage from the LM3445/48 regulator. Both the VCC startup current and discharging of the EMI filter capacitance for proper phase angle detection are handled by Q1. Therefore Q1 has to block the maximum peak input voltage and have both sufficient surge and power handling capability with regards to its safe operating area (SOA).

A minimum value of 13V is recommended for V_{AUX}. Solve for auxiliary turns count in the following manner.

$$\left(\frac{V_{AUX}}{V_{OUT}} \right) = \left(\frac{N_{AUX}}{N_{OUT}} \right)$$

OVERVOLTAGE PROTECTION

(OVP) in case of LED open circuit failure. The use of this circuit is recommended for stand-alone LED driver designs where it is essential to recover from a momentary open circuit without damaging any part of the circuit. In the case of an integrated LED lamp (where the LED load is permanently connected to the driver output) a simple zener diode or TVS based overvoltage protection is suggested as a cost effective solution. The zener diode/TVS offers protection against a single open circuit event and prevents the output voltage from exceeding the regulatory limits. Depending on the LED driver design specifications, either one or both techniques can be used to meet the target regulatory agency approval.

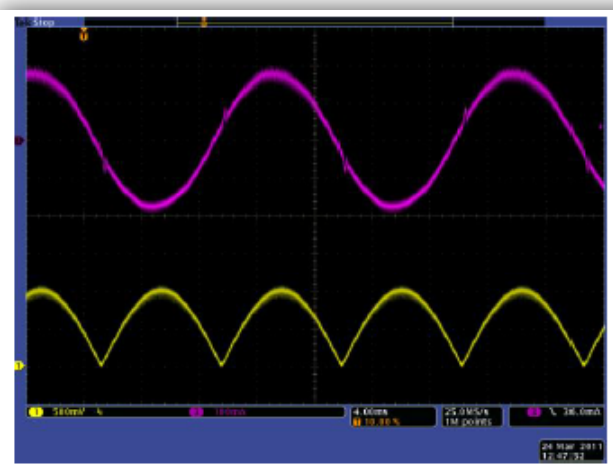


The OVP threshold is programmable and is set by selecting appropriate value of zener diode D13. The resistor capacitor (R19, C15) combination across the base of transistor Q5 is used to filter the voltage ripple present on the auxiliary voltage and prevent false OVP tripping due to voltage spikes caused by leakage inductance. The circuit operation is simple and based on biasing of transistor Q5 during fault conditions such that it pulls down the voltage on the FLTR2 pin to ground. The bias current depends on how much overdrive voltage is generated above the zener diode threshold. For proper circuit operation, it is recommended to design for 4V overdrive in order to adequately bias the transistor. Therefore the zener diode should be selected based on the expression:

$$V_Z = \left(\frac{N_{AUX}}{N_{OUT}} \right) \times V_{OVP} - 4V$$

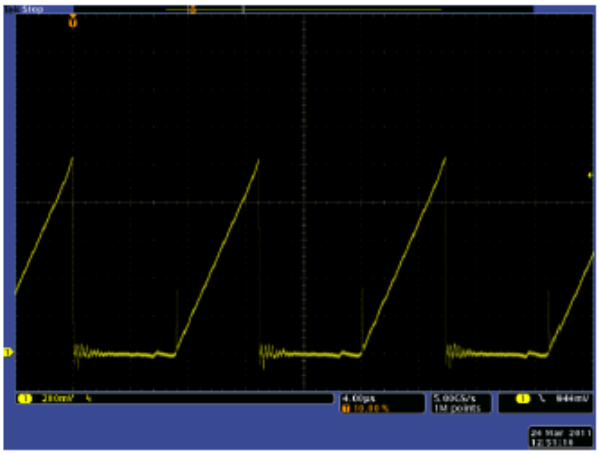
where, V_Z is the zener diode threshold, N_{AUX} and N_{OUT} are the number of transformer auxiliary and secondary turns respectively, and V_{OVP} is the maximum specified output voltage.

LM3445 Flyback Steady State Operation



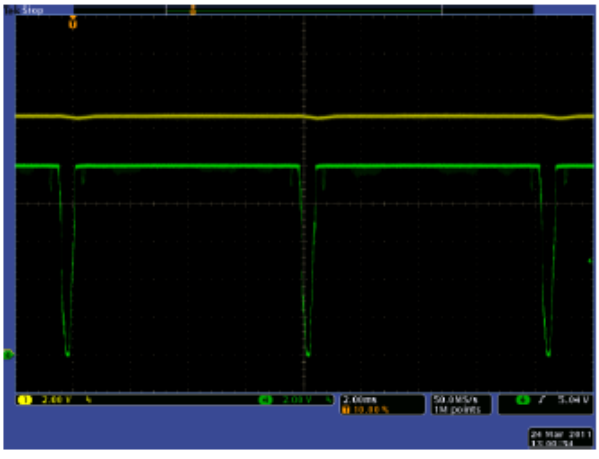
Ch1: FLTR2 Voltage, Ch3: Input current

Ch1: MOSFET Q2 Drain Voltage

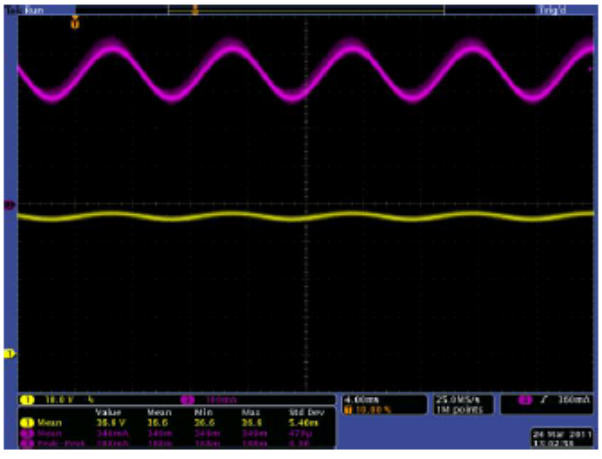


Ch1: ISNS Voltage

Ch1: Auxiliary winding voltage (T1 – pin4)

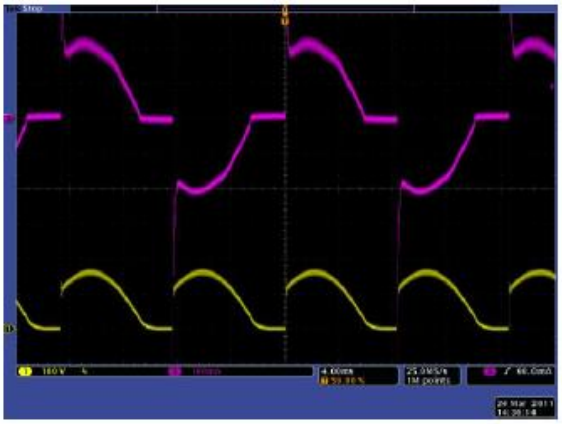
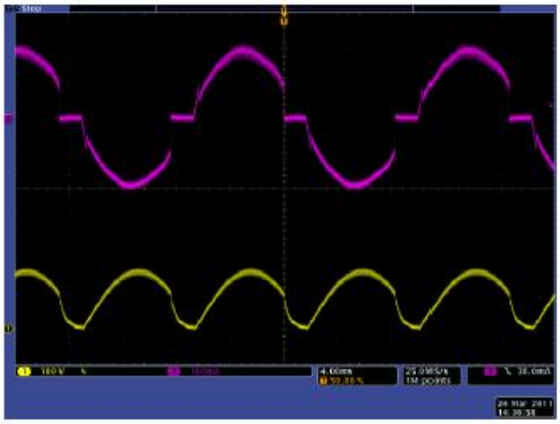
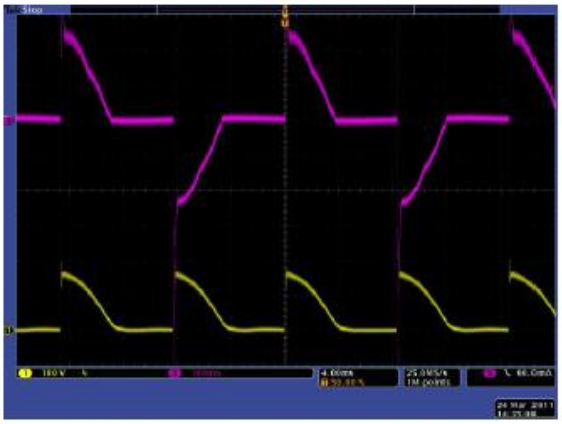
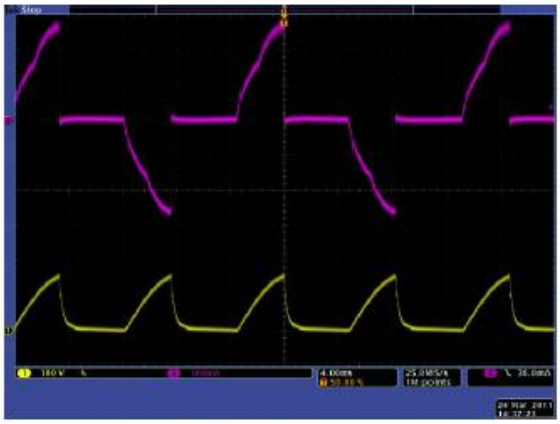
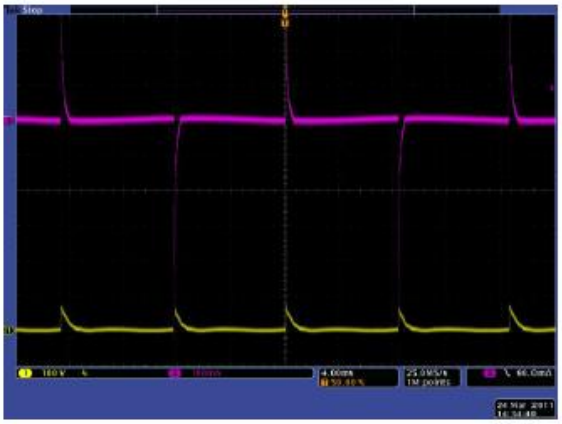


Ch1: VCC Voltage, Ch4: BLDR Voltage



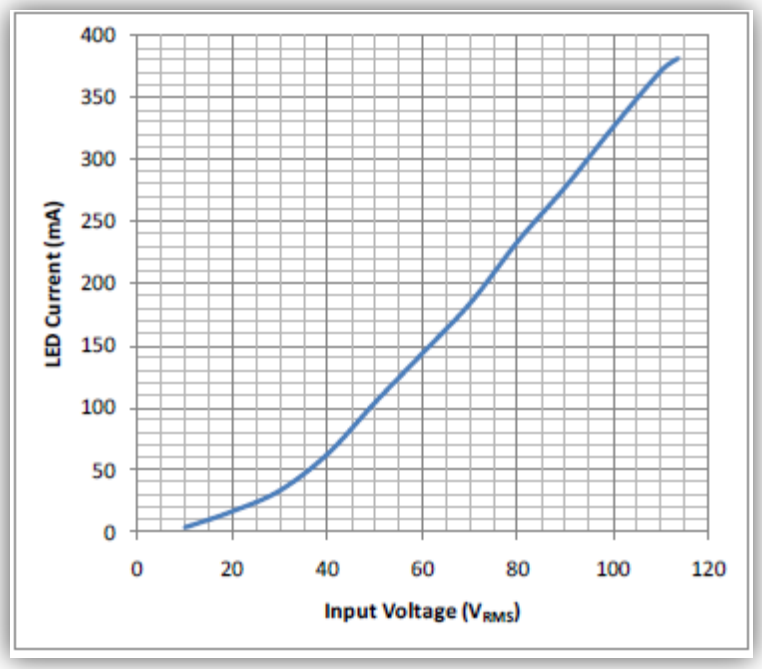
Ch1: Output voltage, Ch3: LED current

LM3445 Flyback Dimming Operation

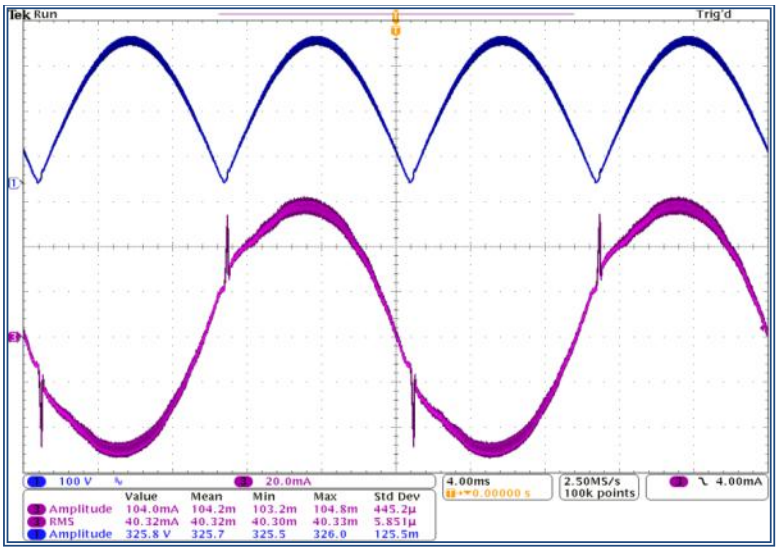
Forward Phase Dimmer	Reserve Phase Dimmer
	
Ch1: Input Voltage; Ch3: Input Current	Ch1: Input Voltage; Ch3: Input Current
	
Ch1: Input Voltage; Ch3: Input Current	Ch1: Input Voltage; Ch3: Input Current
	
Ch1: Input Voltage; Ch3: Input Current	Ch1: Input Voltage; Ch3: Input Current

LM3445 Flyback Dimming Operation - Cont

Input Voltage (V_{rms})	Input Power (W)	Output Voltage (V)	Output Current (mA)	Output Power (W)
113.6	16.27	36.43	380.8	13.87
110	15.72	36.3	370.5	13.44
100	13.55	35.9	325.5	11.68
90	11.39	35.51	277.6	9.85
80	935	25.08	233.8	5.86
70	7.19	34.47	184.1	6.34
60	5.48	33.91	143.9	4.87
50	3.85	33.23	104.2	3.46
40	2.24	32.38	62.7	2.03
30	1.14	31.3	33.3	1.04
20	0.58	30.38	16.5	0.50
10	0.14	28.81	3.5	0.100

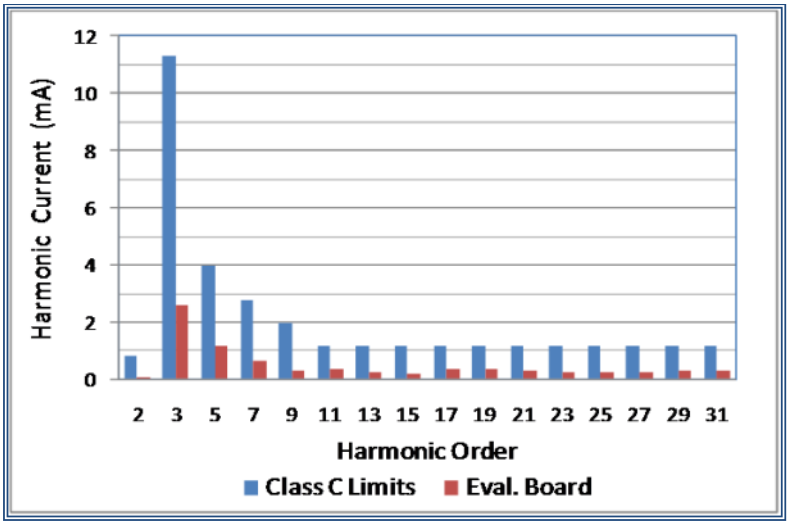


LM3445/48 Isolated Design THD & PF Analysis



Measured Power Factor = 0.94

Constant frequency DCM operation with AC line injected into FLTR2

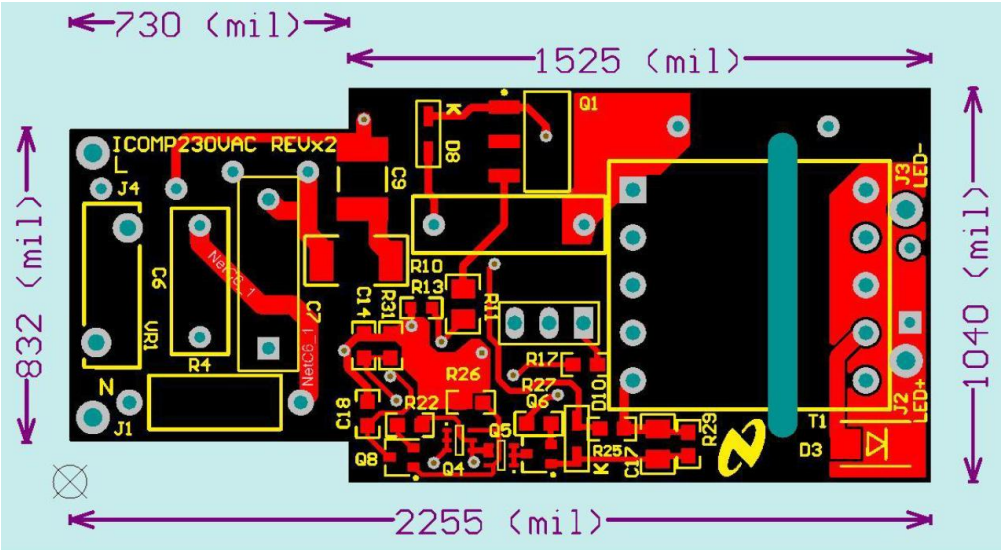


Measured THD = 7.8 %

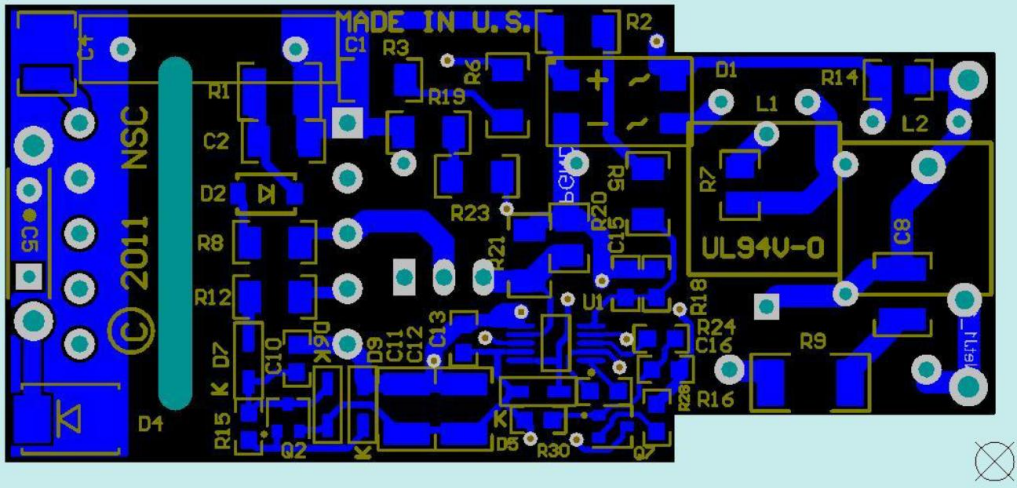
PF consist of AC current lead/lag plus distortion factor. AC current is in phase with AC voltage, and very small amount of distortion

LM3445 Isolated Flyback PCB Layout

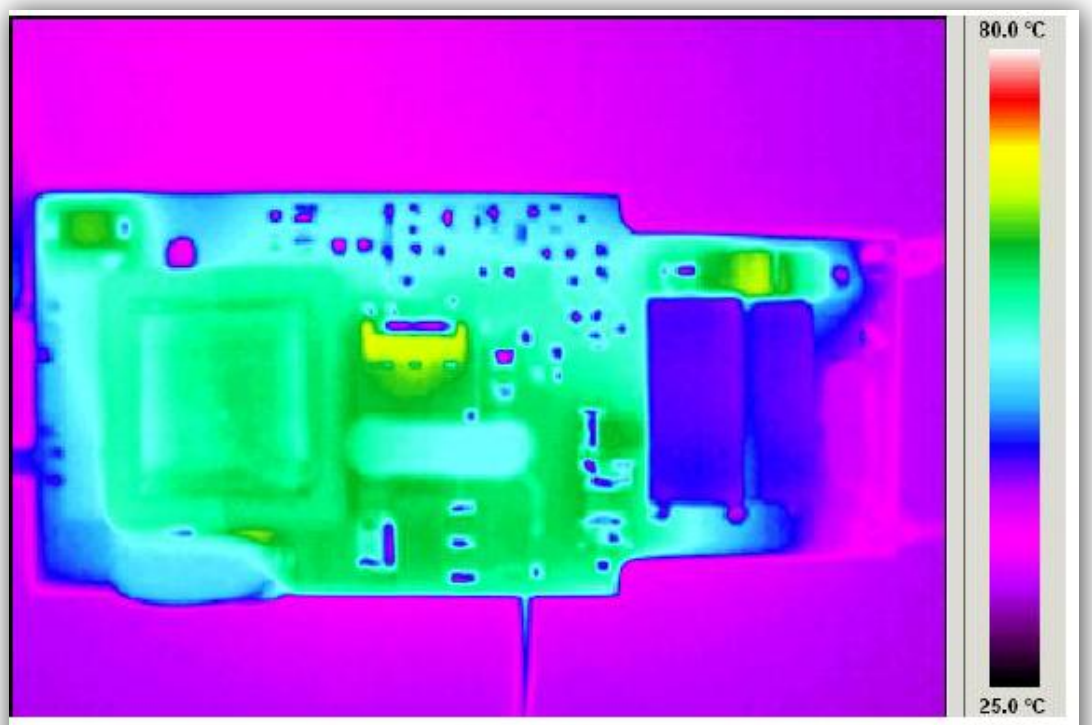
Top Layer



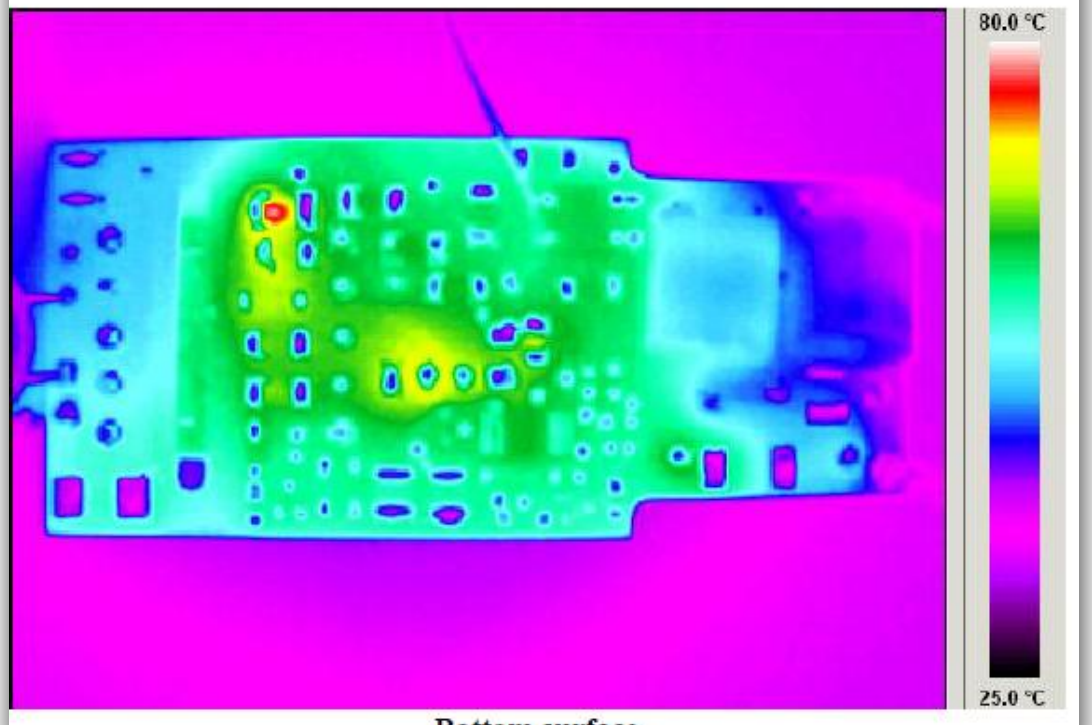
Bottom Layer



LM3445 Isolated Flyback PCB Thermal Images

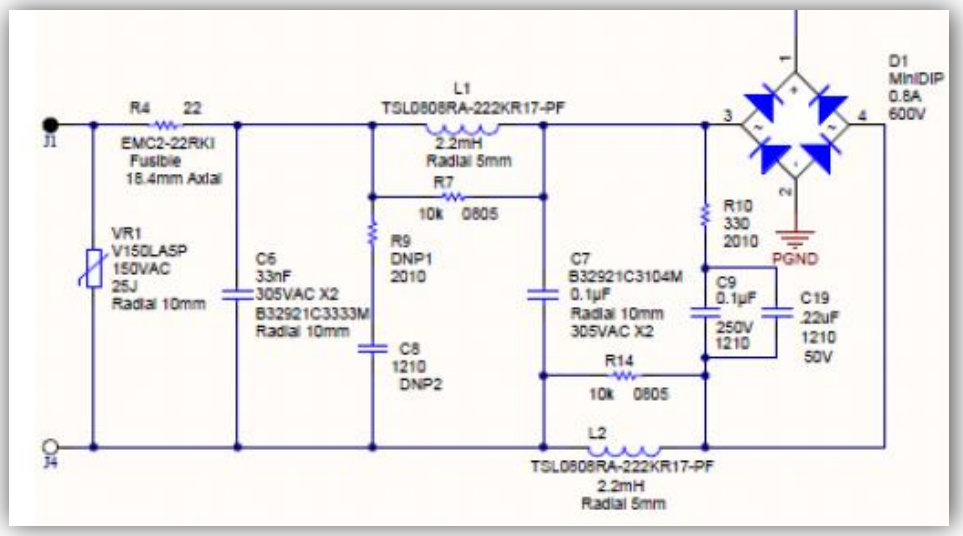


Top surface

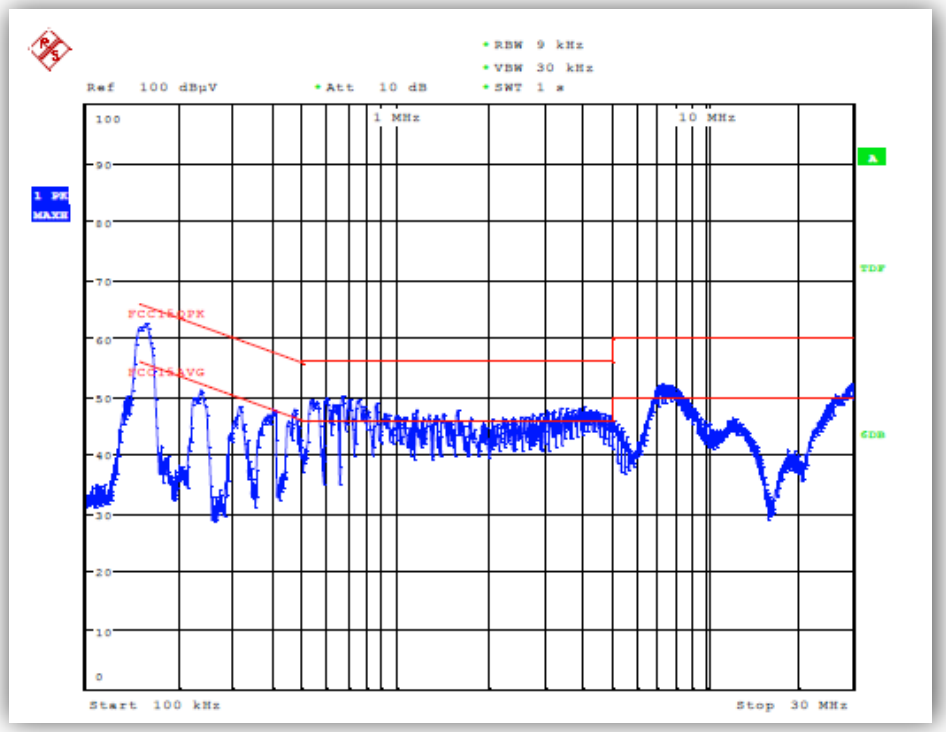


Bottom surface

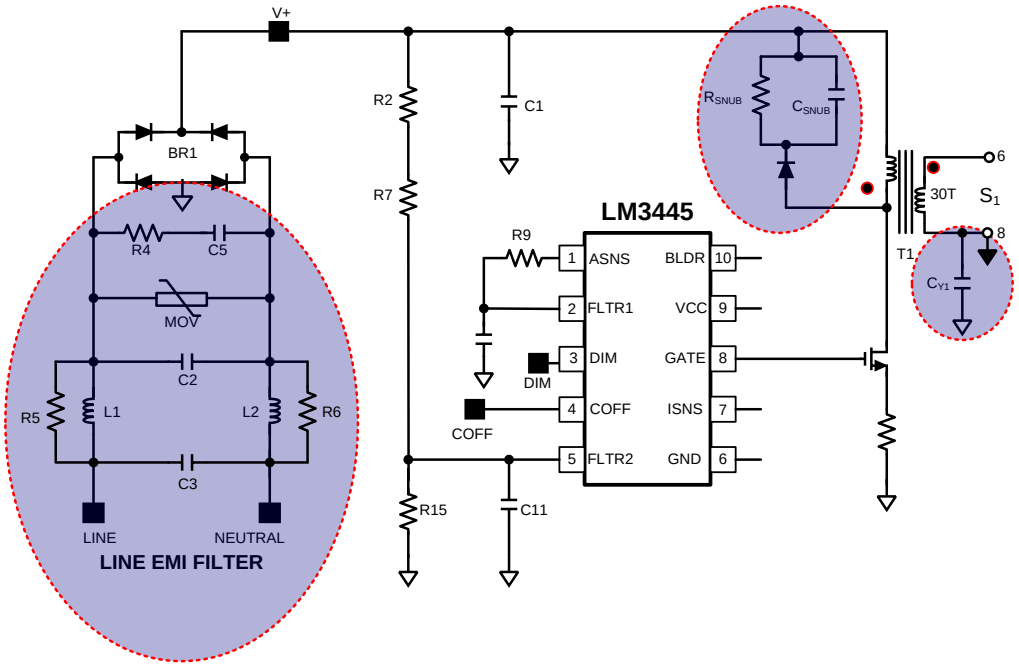
LM3445 Isolated Flyback EMI Scans/Results (Po > 12W)



LM3445 Flyback E1I scan



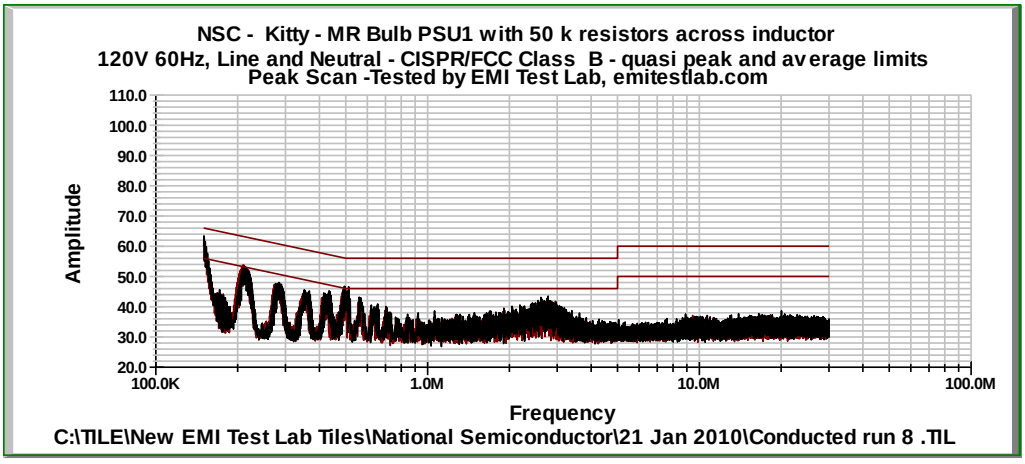
EMI Filter Schematic – Alternative Design (P_{OUT} < 12W)



EMI Filter BOM – Alternative Design

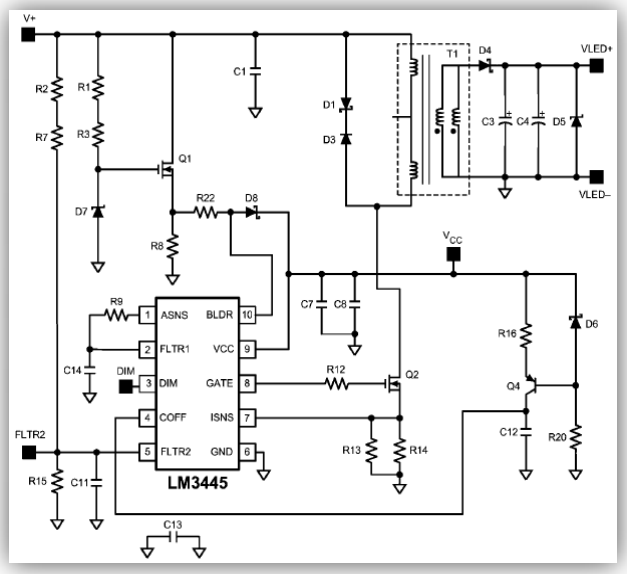
C3	0.01uF	X2-Cap
C2	0.1uF	X2-Cap
L2	4.7mH	Radial
L1	4.7mH	Radial
R4	430Ω	2512
C5	0.33uF	1808 250V
C1	47nF	630V
CY1	??	??

Conducted Emissions – Alternative Design



LM3445 Flyback Feed-Forward Circuit Analysis

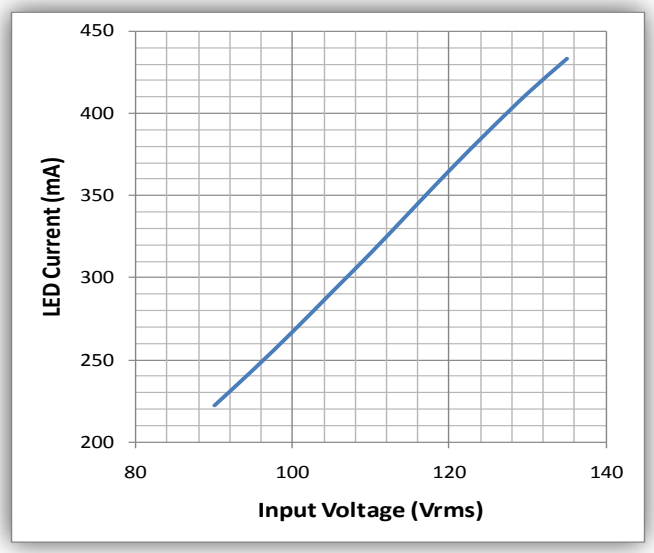
Typical LM3445 schematic w/o Feed-Forward circuitry



By injecting in a small portion of the rectified AC input waveform into FLTR2 of the LM3445/48 you essentially create an open loop power factor controller. The circuit regulates input current, and if the AC voltage remains constant, you have created an input power regulated converter. The output power is always constant and equal to the input power times the efficiency of the converter.

An issue can be seen if the input voltage changes, the output current will also change. The following circuit creates a feed-forward mechanism to counter the input voltage changes.

Typical LM3445 line regulation w/o Feed-Forward circuitry



LM3445 Flyback Operation w/o Feed-Forward

- Fixed off-time based on R16 and C12
- Fixed on-time based on primary inductance (Lp), R13//R14 and VFLTR2
- Constant duty cycle (D) operation in DCM operating mode
- Power input proportional to square of input RMS voltage

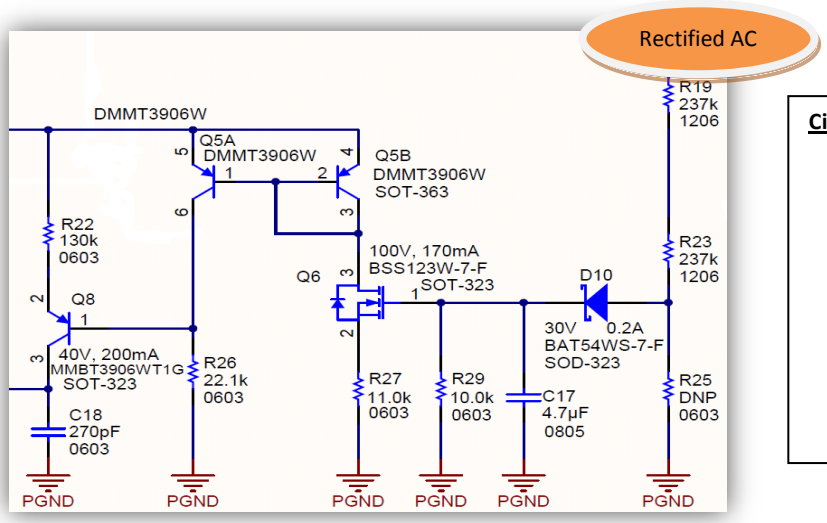
Input power programmed by external component values

LED current varies + 18%,– 40% with input RMS voltage

The schematic and data above explains one of the design considerations when using the LM3445 in an isolated topology. The LM3445/LM3448 regulates input AC current. If the line voltage is consistent, one could say it regulates input power. Output power is simple input power multiplied by the converters efficiency. Output power is the Led stack voltage multiplied by LED forward current. If either variable moves up/down, the other variable will move down/up to keep the output power consistent. By feeding in a portion of the AC waveform into FLTR2, any increase/decrease on the line voltage will be seen as a change in the LM3445/48 internal reference (FLTR2). This then changes the regulation point on the primary, and consequently the LED current will vary. Most line voltages do not realistically vary by more than 5%, and no feed-forward line voltage circuitry is required. However if it were required a circuit is now described to tighten the line regulation up.

LM3445 Flyback Feed-Forward Circuit Analysis - Cont

The idea of this circuit is to change the off-time of the LM3445 (controls input power) as the line varies



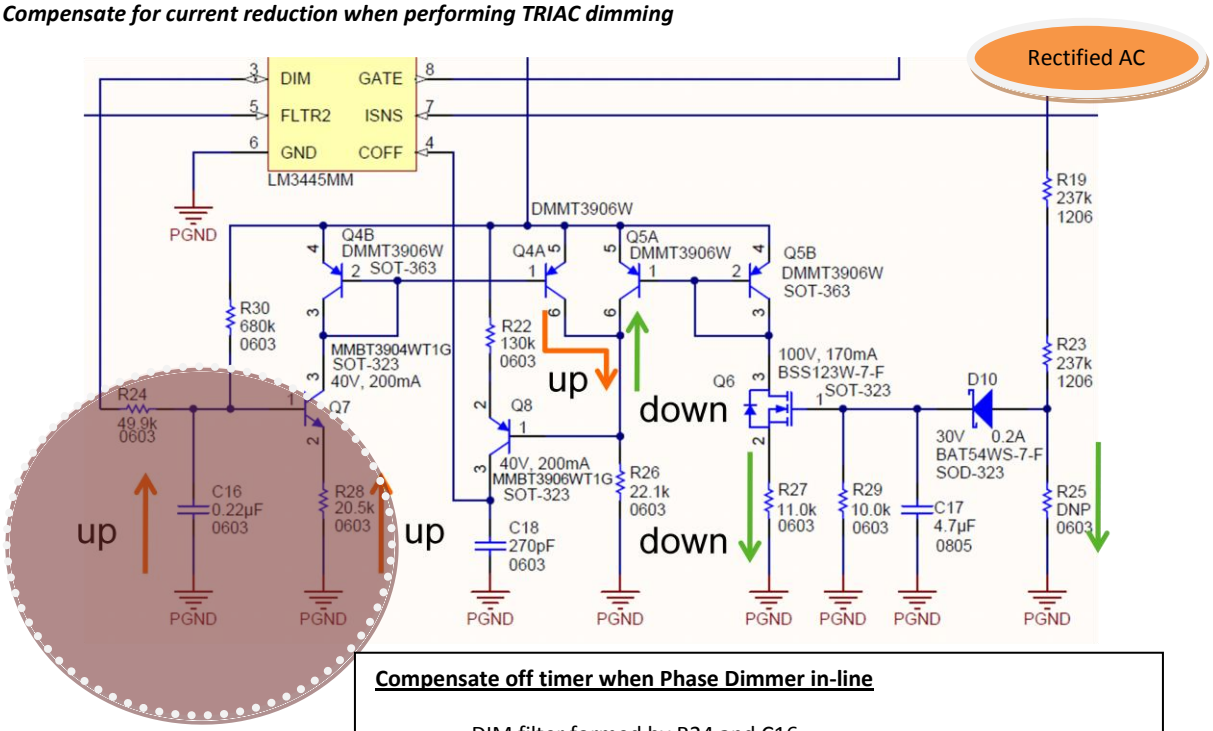
Circuit operation

- Input voltage divider based on R19, R23 and R29
- Low pass filter formed by R29 and C17
- Voltage to current converter formed by Q5, Q6, Q8, R27 and R22
- Off-time based on I_{C18} and C18

Problem:

Circuit cannot differentiate between input voltage variation due to line fluctuation and TRIAC dimming

- TRIAC dimming → Reduced input voltage → Reduced Q5 current → Increased I_{C18} current → Reduced T_{off}
- ***Compensate for current reduction when performing TRIAC dimming***



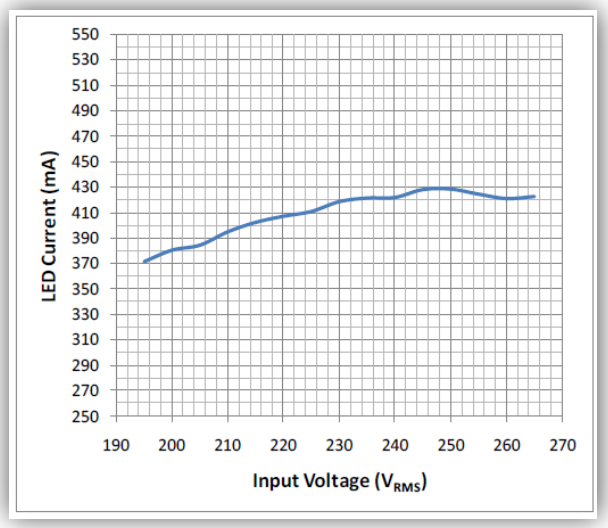
Compensate off timer when Phase Dimmer in-line

- DIM filter formed by R24 and C16
- Correction current set by R28

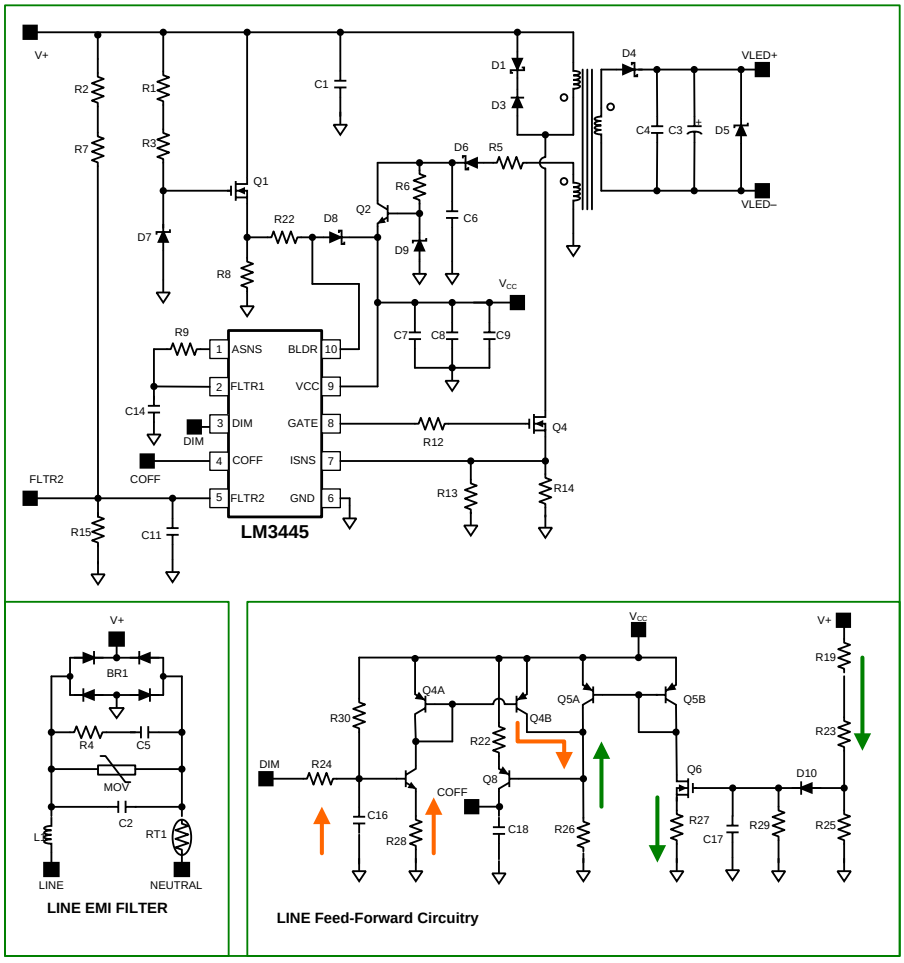
Tuning

- Large R28 results poor dimming ratio
- Small R28 results in flicker at low dimming level

LM3445 line regulation with Feed-Forward circuitry



LM3445/48 Line Feed-forward Schematic

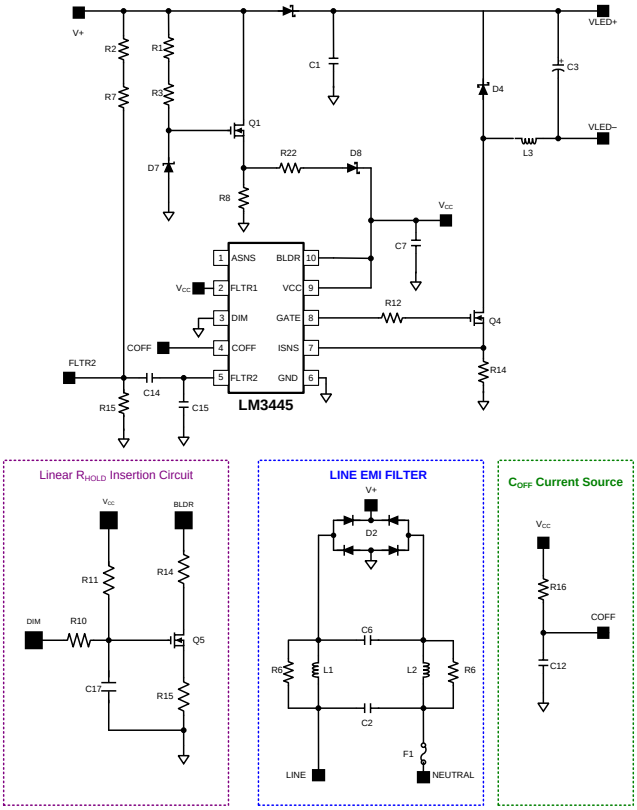


AC/I_{LED} Non-isolated Buck Topology with line injection

The following buck topology operates same/similar to the flyback topology previously mentioned. Remember, a Buck-Boost is simply a non-isolated Flyback. The method of injecting a small portion of the AC line voltage into FLTR2 pin works in the non-isolated buck and buck-boost topologies. One also sees that this design is simpler than the previous Buck topology; the external component count is greatly reduced. This

LM344548 AC/I_{LED} with line injection Buck Topology evaluation boards

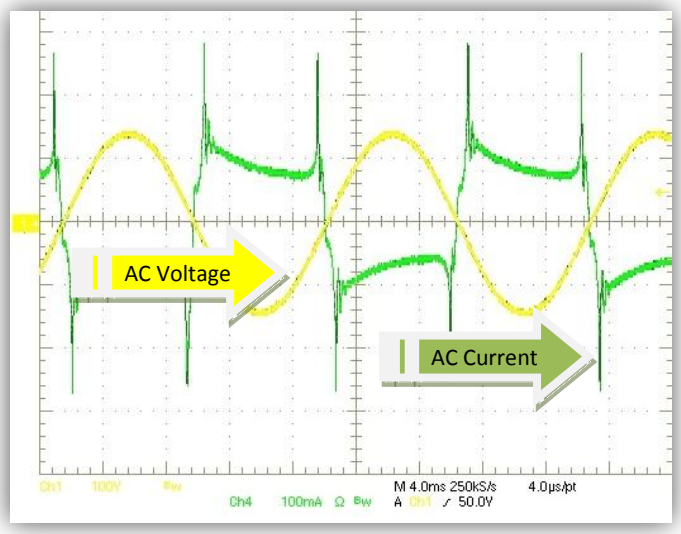
- **Strengths**
  - Low Cost
  - Small solution size
  - Acceptable dimming ratio (40:1)
  - Good efficiency when optimized (eff > 80%)
- **Weakness**
  - Not isolated
  - Better with higher LED stack voltages
  - 120Hz ripple magnitude depends on size of output electrolytic

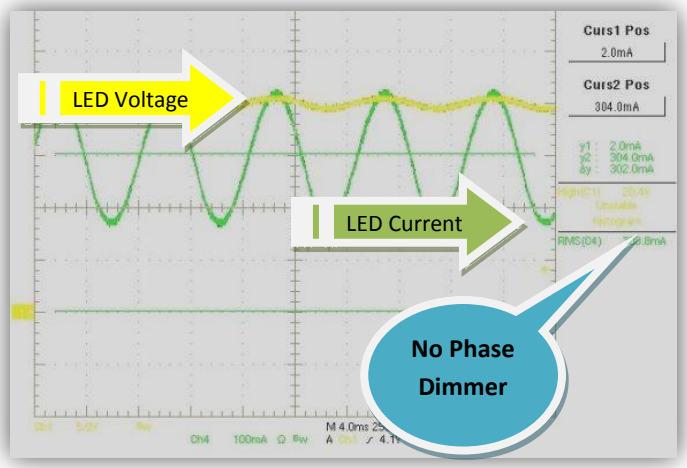


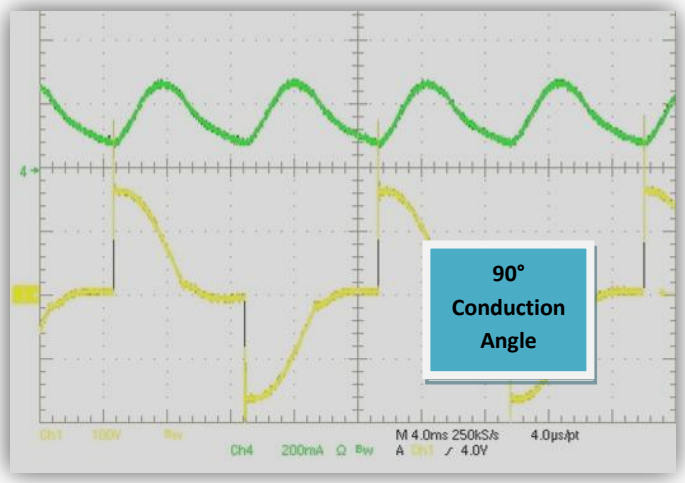
This architecture relies on shaping the input current to ensure good triac/SSL lamp compatibility. By injecting a portion of the AC waveform into the FLTR2 pin current is increased at the beginning and at the end of the AC phase dimmed cycle. From our experience in our laboratory we know that common phase dimmers have firing and holding current issues in these two areas.

The previous schematic shows a “Linear Hold” circuit described in the previous architecture. This circuit can be used with any LM3445 circuit where low conduction angle (low dimming) issues are observed.

AC/I_{LED} Non-isolated Buck Topology with line injection AC Waveforms

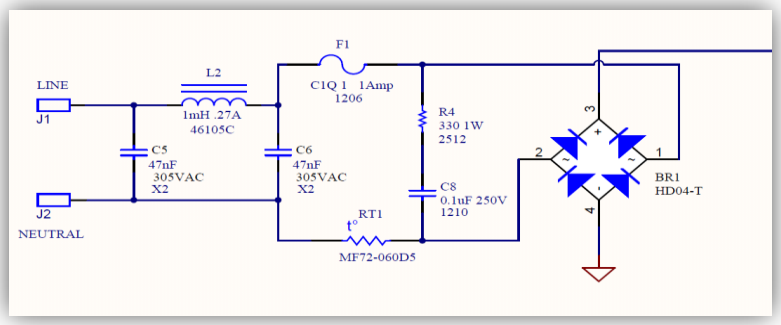




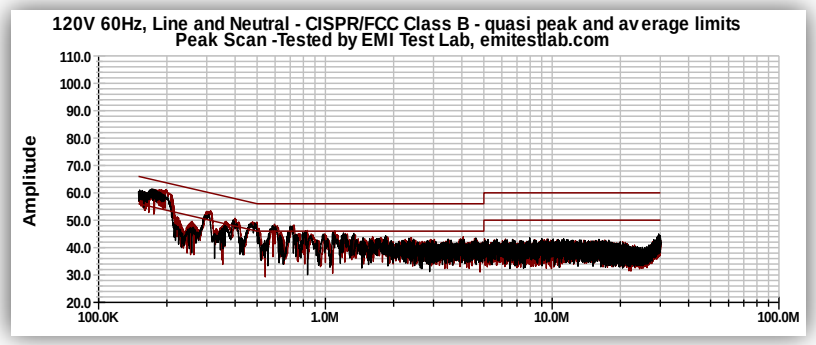


LM3445/48 Non-Isolated Buck (line injection) EMI Analysis

EMI Filter Tested



EMI Scan Results



	Freq	Ave limit	Ave Measurement	Delta below limit
Line	198 kHz	54	50.3	-3.7
Neutral	198 kHz	54	49.5	-4.5
Line	302 kHz	50	42.5	-7.5
Neutral	302 kHz	50	41	-9
Line	403 kHz	48	37	-11
Neutral	403 kHz	48	38	-10
Line	488 kHz	46	35	-11
Neutral	488 kHz	46	36	-10

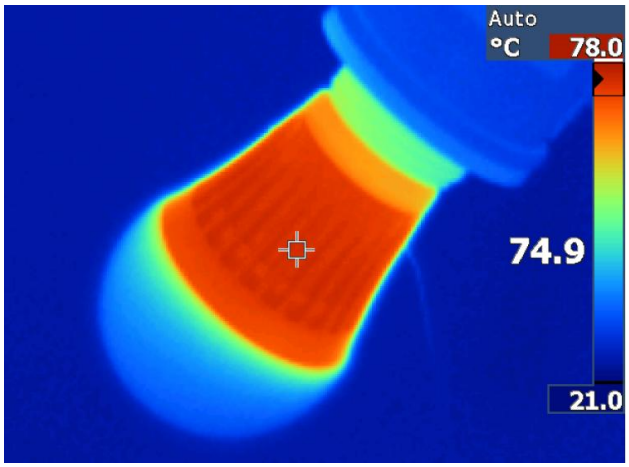
Understanding the Results

- For the initial EMI scan a peak measurement is taken as it is a much faster scan process.
- If the scan using the peak measurement passes the average limit, it is definitely a pass
- Any points above the average limit on peak are checked again using a different receiver which performs an average measurement – these measurements are shown above.
- EMI scans of the LM3445 will typically have an average reading lower than the peak because the switching frequency is constantly changing – it is a spread spectrum effect.
- Our worst case point was 3.7dB under the average limit. To put this in perspective, if we were 6dB under our noise level would be half of the maximum allowed.

Thermals

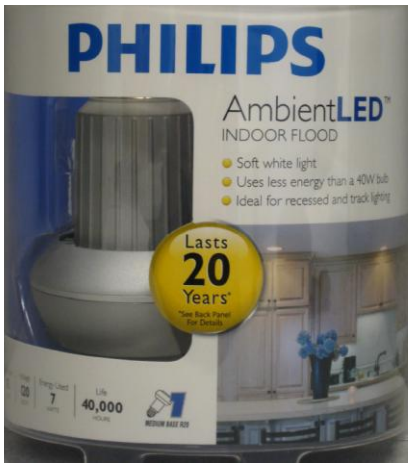
Product from Lighting Science

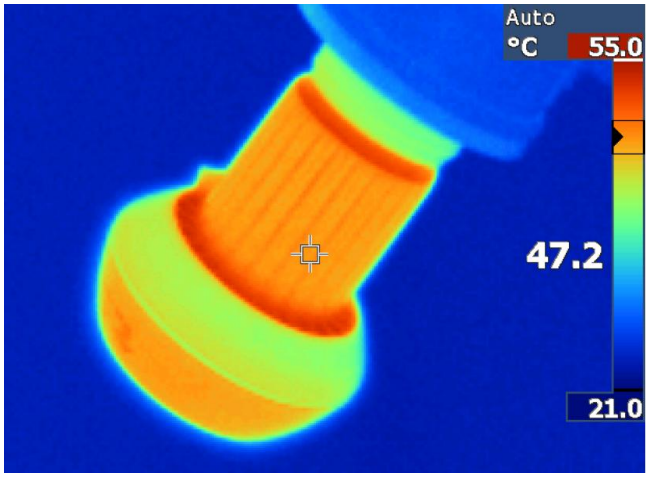
- 50,000 hours life
- 5 year warranty
- Dimmable
- 429 Lumens
- 8.6 Watt
- Efficacy: 49 lm/watt
- CRI: 85
- Light color: 3032 (bright white)
- UL, RoHS & FCC mark



Philips LED

- 40,000 hours life
- Lasts 20 years - (3~4 hours/day)
- 155 Lumens
- 7 Watt
- Light color: 3100 (soft white)
- UL & FCC mark





EMI Filter Design

The LED lamp drivers are required to comply with conducted and radiated EMI limits defined in FCC CFR Section 15 (USA), CISPR-15 (Europe) or other equivalent region standard. Input EMI filters are used in conjunction with power stage to reduce the noise generated by high frequency switching sequence. The filter configuration and performance is dependent on various product parameters such as the target power levels, the size and target cost of the solution, the isolation requirements, the enclosure specification and the input power line connection. For integrated LED lamps, the size and cost of the solution generally dictate the filter configuration. Further, the absence of earth ground connection in Edison, E27 or Bayonet bases and phase dimming requirements demands a different approach to filter design then used for conventional AC-DC PFC topologies. Based on the familiarity of EMI filter techniques, some of the major differences between conventional topologies and phase dimmer compatible topologies are highlighted in this section. A brief overview of design philosophy and simulation design aid is also presented.

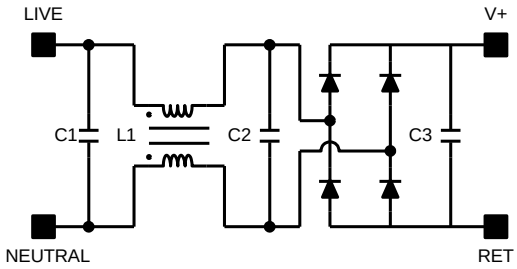


Fig. 1: Conventional EMI filter configuration.

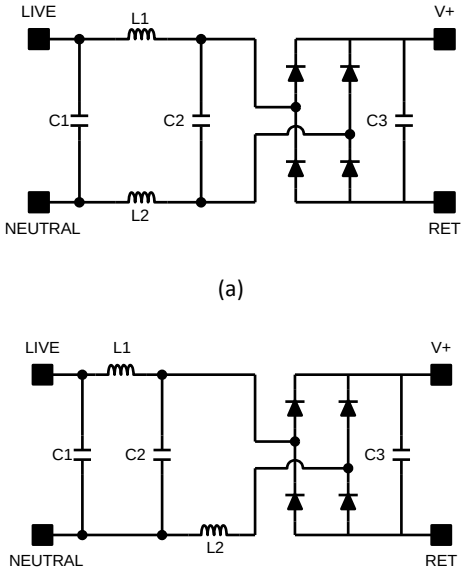
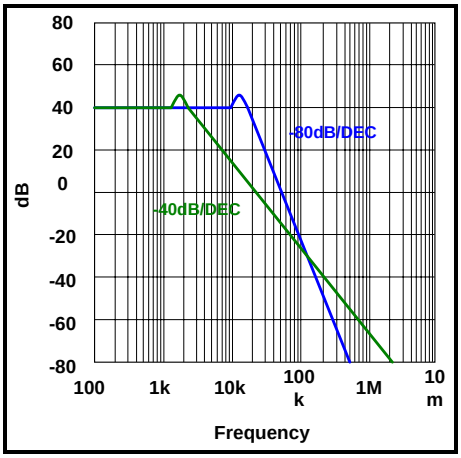


Fig. 2: LED driver EMI filter configuration; (a) 2nd order filter, (b) 4th order filter.

4th order and 2ND order bode Plot



Common EMI Filter Configurations

The conventional EMI filter shown in Fig. 1 typically consists of common mode power line chokes, L1 and X2 capacitors C1 and C2 configured in PI-configuration to form a single section low-pass filter. In contrast, the use of discrete drum core inductors with X2 or high voltage capacitors is preferred in LED drivers in order to meet the stringent size and cost requirements. Based on the LED driver power level, either a second order (Fig. 2(a)) or fourth order filter configuration (Fig. 2(b)) can be employed to attain desired level of attenuation over the frequency range of interest.

It is important to note here that the filter selection and design process is iterative in nature, where it is often required to change the configuration based on the exact nature of EMI signature. Therefore, the choice between conventional topology illustrated Fig. 1 and discrete topologies shown in Fig. 2 is interchangeable. It is also possible to cascade the two or more circuits, if required, to reliably meet the regulatory specifications.

Filter Design Procedure

The traditional approach to EMI filter design consists of measuring or estimating the differential mode and common mode noise generated by the power supply and then calculating the attenuation characteristics required to drop the noise floor across the frequency range below the target specifications. The filter topology and components are selected to match the calculated attenuation characteristics. For large power supplies, it is common practice to select the smaller inductor values and larger capacitor values in order to minimize the volume of the EMI filter. For LED driver solutions the general filter design procedure remains identical, with few modifications necessary to address two wire input connection (no earth grounding) and phase dimming requirements.

For an LED driver with two-wire input connection it is possible to design a differential mode low pass filter capable of reducing the conducted noise in low frequency range (9 kHz to 5 MHz) using circuit configurations shown in Fig. 2. However, for these filters larger inductor values in combination with lower capacitor values are preferred to achieve the desired corner frequency. This change in design procedure is needed to achieve improved compatibility with phase dimmers the details of which are explained in “RC Snubber Design” section. For LED drivers with power levels ranging from 6W to 30W, off-the-shelf through hole and surface mount drum core inductors ranging in value from 1 mH to 4.7 mH are frequently selected. The X2 capacitor value is limited to range between 22nF and 0.1uF due to size limitations. The enclosure dimensions and layout requirements dictate the final design of the differential filter.

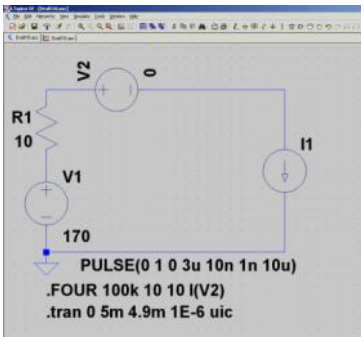
For frequencies greater than 5 MHz, the parasitic components of filter elements start dominating and thereby modifying the attenuating characteristics of the filter. The determination of such parasitic components is often difficult process. Further, at higher frequencies the common mode noise increases beyond the differential threshold and it begins dominating the EMI signature. The absence of earth ground make it difficult to significantly attenuate the common mode noise using traditional circuit techniques such as common mode chokes and Y-capacitors. To control the common mode noise in LED drivers, it is essential to understand the common-mode noise path formed via parasitic capacitances from high dv/dt switch nodes to surrounding ground. Based on the EMI signature, it is required to reduce the magnitude of the noise source or address the coupling mechanism by inserting filter elements such as ferrite bead inductances or snubber circuits. For isolated designs it is also critical to analysis the impact of Y-capacitor across the transformer on common mode noise and to tune the capacitor value to achieve minimum possible noise coupling through LED load. For most designs, the use of common mode chokes between the input ac supply and the driver or between the driver and the LED load is avoided to minimize the size of the filter solution and minimize the cost. The design procedure for higher frequency therefore deviates from the known filter design techniques to more iterative process in order to achieve noise attenuation between 5 MHz and 30 MHz frequency range.

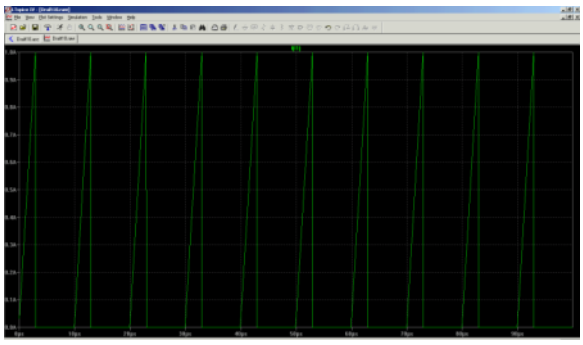
Filter Design using SPICE Simulator

Selection of EMI filter topology and design iterations can be performed using SPICE simulation tool. To achieve good correlation between simulation and experimental data, it is essential to accurately model the noise source within the power converter. In the example shown below, the worst case differential noise through the DCM Flyback converter is modeled using an ideal current source. Once the noise source is known, the filter design process can be performed in following steps.

1. Calculate the Fourier series component of noise source using SPICE .FOUR command.
2. Estimate the magnitude of the noise sensed by the LISN using the formula,
$$V_{LISN,\{i\}} = 50 I_{N,\{i\}} \text{ where } i = 1, 2 \ldots n \text{ harmonics.}$$
3. Convert the LISN voltage to dBµV in order to compare it with regulatory limits,
$$V_{LISN,\{i\}}(dB\mu V) = 20\log\left(\frac{V_{LISN,\{i\}}}{10^{-6}}\right).$$
4. Determine the attenuation required by subtracting the noise magnitude from specified limit,
$$F_{A,\{i\}}(dB) = V_{LISN,\{i\}}(dB\mu V) - V_{LIMIT,\{i\}}(dB\mu V)$$
5. Select the filter topology and corner frequencies to achieve calculated attenuation.

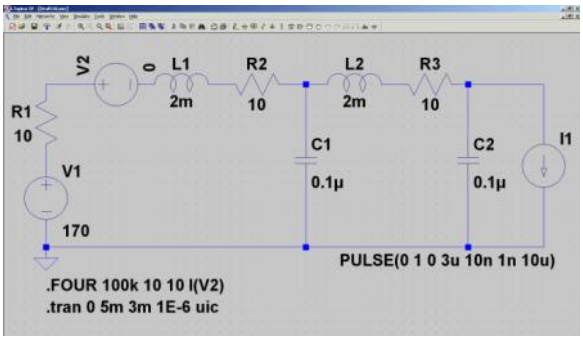
Differential Mode Noise Estimation

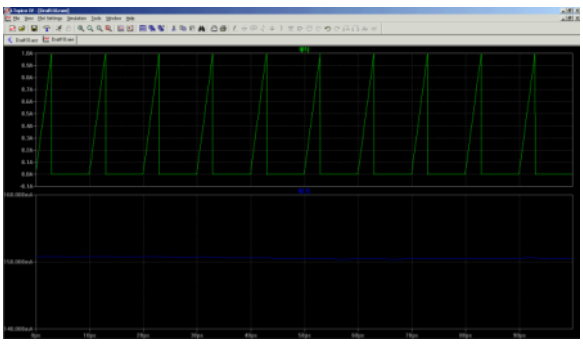




Harm.	Freq. kHz	Current mA	LISN V	Noise dBµV
1	100	272.6	13.63	142.7
2	200	199.6	9.98	140
3	300	117.1	5.855	135.4

Differential Mode Filter Design



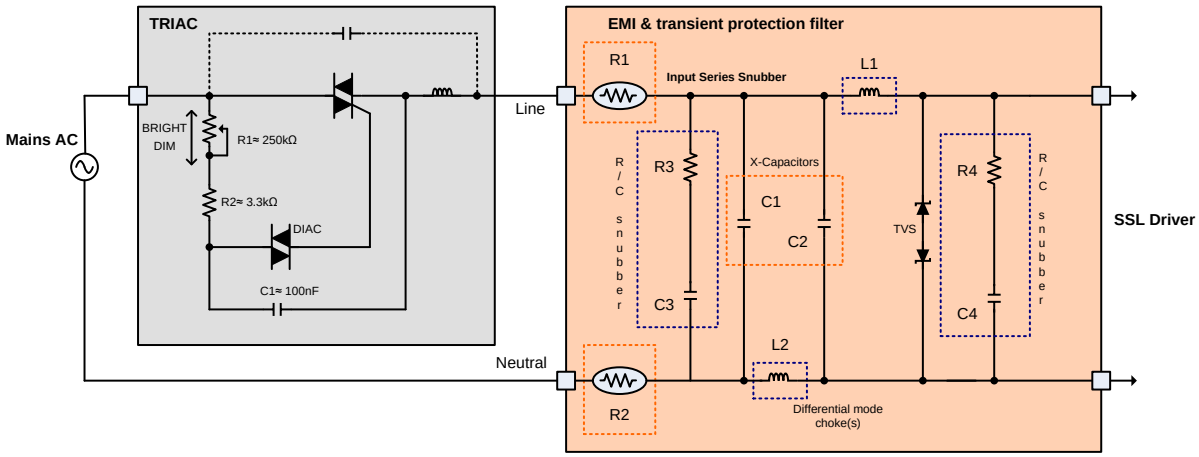


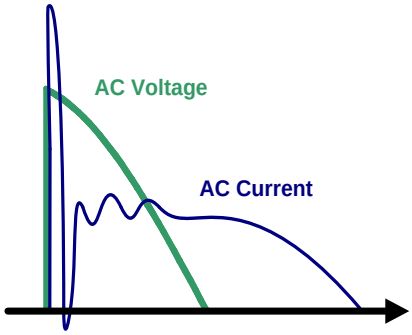
Harm.	Freq. kHz	Current µA	LISN mV	Noise dBµV
1	100	50.38	2.519	68.02
2	200	4.585	0.229	47.21
3	300	1.914	0.096	39.62

EMI Misc

A " Y" rated AC capacitor from the primary ground to the secondary ground is also critical for reduction of common mode noise. The combination of filters along with any necessary damping can easily provide a passing conducted EMI signature.

Resistor/Capacitor Front End Snubber Network Design





One of the two main technical challenges mentioned when mating SSL solutions with phase dimmers is the harsh turn on/off of the phase dimmer, and its reaction with reactive components within the EMI filter of the driver. The illustration to the left illustrates the challenge. High dv/dt of the phase dimmer causes a high di/dt of the AC input current. This coupled with capacitors and inductors (C1, C2, L1, L2) within the EMI filter allow the input current to ring below 0A, and this will certainly turn-off or miss-fire the triac within the dimmer.

AC Inrush Damper Circuits

The inrush spike can also excite a resonance between the input filter of the TRIAC and the input filter of the converter. The associated interaction can cause the current to ring negative, as shown in the above illustration, thereby shutting off the TRIAC. A TRIAC damper can be placed between the dimmer and the EMI filter to absorb some of the ringing energy and reduce the potential for misfires. The damper is also best sized experimentally due to the large variance in TRIAC input filters. By adding resistor and series capacitors across the AC line, and add input series resistors. One should only add these components if necessary. Both solutions will decrease the system efficiency, especially the input series resistors (R1 & R2). Keep these values as low as possible.

Reference	Range of Values
R1 & R2	5Ω - 15Ω Po > 10W
R1 & R2	5Ω - 33Ω Po < 10W
R3 & R4	220Ω - 1kΩ
C3 & C4	0.1uF – 0.33uF (250V min)

NOTE: Be selective with the type of capacitor is used for C3 & C4. SMT is not a good choice due to reliability issues. Thru-hole polyester or safety capacitors are recommended. Safety capacitors are not mandatory due to the fact that there is a resistor in series with the capacitor(s). Pulse rated or fused resistors are a good choice for resistors R1 & R2.

Design of Damping Circuits for Input EMI Filter

The impact of the input filter on power supply performance has been widely studied and described in literature. Various damping circuits have been proposed to prevent the filter resonance from degrading the stability of the control loop of DC-DC power converters. In contrast, damping of the input EMI filter in AC-DC power factor corrected (PFC) converters is not considered critical due to the slow regulation bandwidth of the voltage feedback loop. Any disturbance caused by filter resonance does not impact output regulation of the PFC converter as it is damped by the feedback loop. However, inserting such an un-damped EMI filter into a dimmable LED lamp generally leads to visible light flicker and poor light output quality. The degradation in performance is caused by the interaction between the TRIAC-based dimmer circuit and the EMI filter resonance. In this section, the EMI filter response to TRIAC dimmer output is briefly analyzed and circuits to improve LED driver and dimmer compatibility are presented.

Understanding TRIAC Dimmer and EMI Filter Interaction

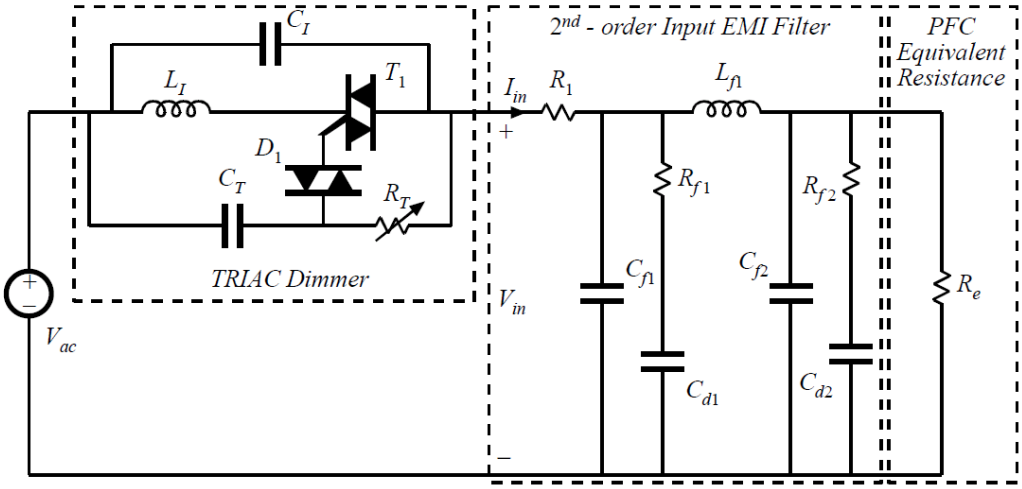


Fig. 1: Low frequency equivalent circuit model consisting of a series connected TRIAC dimmer, an input EMI filter and power factor corrected LED driver.

The AC equivalent circuit diagram of the system is shown in Fig. 1. For the purpose of this analysis, the high frequency behavior of the AC-DC PFC rectifier is neglected and the complete power stage is modeled as an equivalent resistance, Re, give by

$$R_e = \frac{V_{ac,rms}^2}{P_{in}}$$

where, P_{in} is the total input power drawn by the LED driver. From the model, it is clear that better compatibility with the TRIAC-based dimmer is achieved by performing resistor emulation using a PFC loop and maintaining the latching and holding current requirements during the line cycle. However, any perturbations that causes the input current, I_{in}, to drop below holding value threshold can result in

TRIAC misfire and create light flicker. It is therefore required to understand and analyze the transient behavior of the system and its response to the TRIAC firing sequence.

Parameter	Value
V_{ac}	230 V_{RMS}
P_{in}	9 W
R_e	5.88 kΩ
L_I	250 µH
C_I	100 nF
C_{f1}	4.7 nF
L_{f1}	4.7 mH
C_{f2}	33 nF

Table. 1: Input filter circuit components

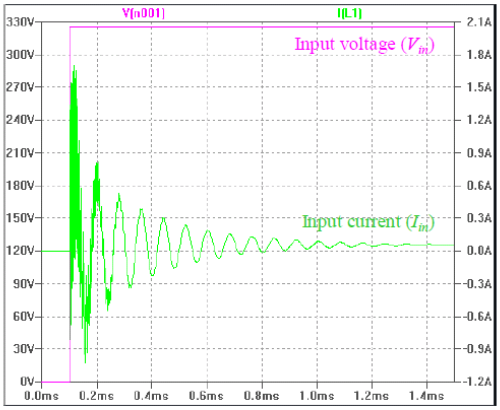


Figure. 2: Undamped input filter response to step voltage transient

To simplify analysis, the response of the behavioral model to step input voltage transients is simulated using SPICE. For an un-damped input filter, as described in Table 1, the response to a step transient generated by an ideal voltage source is shown in Fig. 2. The input current, I_{in}, can be observed to oscillate at frequencies close the resonant frequencies of the filter. Further, the current is found to undergo multiple zero crossings before settling to a steady state value. When operating with a dimmer, such behavior can result in TRIAC commutation causing the input voltage to collapse and interruption of power to LEDs. Multiple TRIAC misfires can manifest as visible flicker and cause damage to both the dimmer and the LED driver circuits. To reduce the magnitude of input current oscillations a suitable damping circuit is required to limit the Q-factor of the input filter. A conventional technique for designing a damping circuit is based on a stability analysis that considers the impedance inequalities between the output of the filter and the input of the power supply. However, optimal design of the damping network based on such impedance inequalities leads to unsatisfactory performance of the LED driver as it does not consider the impact of large input voltage transients. To satisfactorily address the current requirements of a TRIAC based dimmer, it is necessary to investigate damping network design from input transient perspective.

Damping Circuit Design

The damping circuit for an input EMI filter is shown in Fig. 1 and consists of input inrush resistor, R_1, and R-C snubber circuits, R_{f1}, C_{d1} and R_{f2}, C_{d2}. The snubber R_{f1}, $C_{d1}$is used to damp the parasitic inductances and R_{f2}, C_{d2} is used to damp the EMI filter section. The design of the damping circuit is challenging as it involves balancing various conflicting specifications such as efficiency, power factor, EMI and reliability. As a result, there is no single "cook-book" recipe that will apply to all different filter configurations and different LED driver power levels. Often, the tuning of the damper network becomes an iterative process, starting from an educated guess. The starting estimate for damper values can be achieved using SPICE simulations, as shown in Fig. 3. By observing the current I_{in}, response to step input voltage transient, the design performed can be performed using following steps:

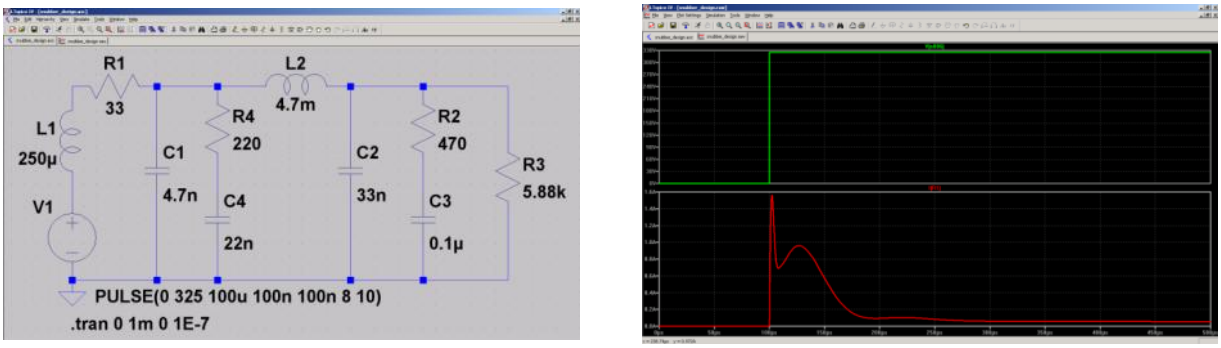


Fig. 3: SPICE simulation setup and simulation results for a step input voltage transient from 0 V to 325 V

1. Select C_{d2} (C3) to be around 3 to 5 times the filter capacitor, C_{f2} (C2). The rule is empirically derived to maximize the effect of damping resistor R_{f2} near the filter L_{f1}, C_{f2} resonance frequency.

2. With just filter L_{f1}, C_{f2} present and C_{d2} selected, tune the resistor value R_{f2} (R2), such that transient input current does not fall below zero for range of input voltages. In most cases, there will be an optimal value of R_{f2}, which will lead to maximum current above zero and minimum ringing. Decreasing the value below the optimal point will cause the current to go negative (over-damped response) while increasing it will cause increased oscillatory response (underdamped response). The choice of R_{f2}, will typically range from 220 Ω to 1 kΩ.

3. Evaluate* the interaction between the estimated parasitic inductance, L_l (L1) (dimmer + transmission wires), and the filter capacitance, C_{f1} (C1) along with the remaining filter components.
   *It is important to note that the estimate of parasitic inductance and its impact on the performance is dependent on various external parameters such as dimmer manufacturers and input voltages ($100V_{RMS}$ (Japan), $120V_{RMS}$ (Americas) and $230V_{RMS}$ (Europe)). Due to higher voltages and therefore lower line currents, interaction between parasitic inductance and EMI filter is found significant only in European dimmers. For Japan and North America, the use of damper R_{f1}, C_{d1}, is optional.

4. Select C_{d1} to be around 3 to 7 times the input capacitor, C_{f1} (C1).

5. Choose the value of R_{f1} (R4) to reduce the ringing associated with the parasitic inductance and the capacitor, C_{f1}. Typically, the value of R_{f1}, is observed to be close to half the value of R_{f2}.

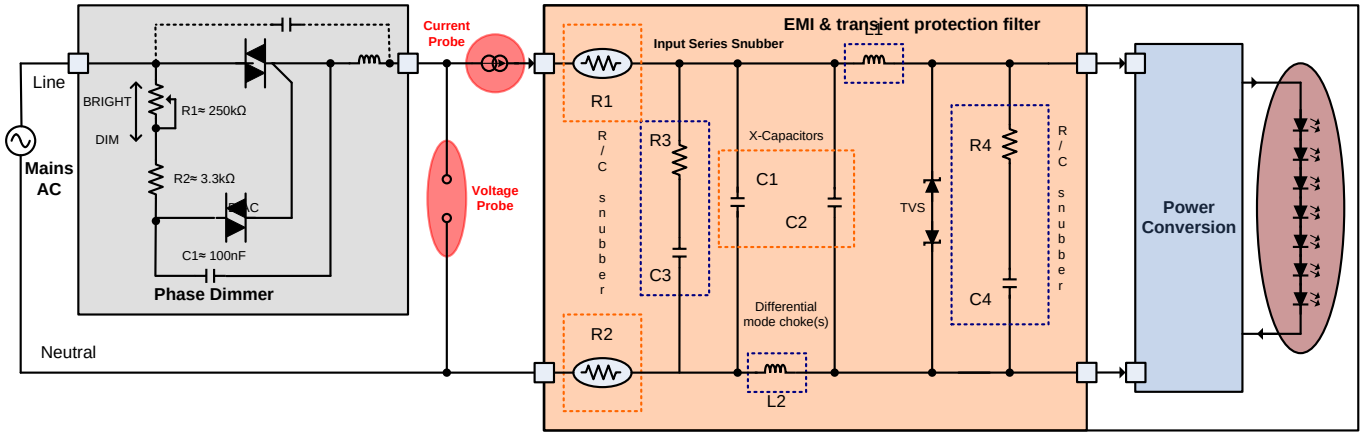
6. Select R_1 (R1) to limit the peak current drawn from the TRIAC to be below 2 A. This will prevent the total instantaneous power drawn from the TRIAC from exceeding its peak ratings (generally 400 VA to 600 VA).

Troubleshooting Phase Dimming SSL compatibility Issues

Now that you have an evaluation PCB or your design I complete its time to optimize its performance. A few common complaints with SSL bulb applications and traditional phase dimmers are:

- Low end dimming flutter
- Flicker (on/off) of the LEDs at various ranges of some dimmers (varies between dimmers)
- Dimming contrast ratio is low

The first step in resolution of the problem(s) is to identify the root cause. Flutter and flicker issues are very common, and the two issues have different roots. First step with identifying the issue is to place an oscilloscope current probe in line with either the line or neutral and a voltage probe across on line/neutral AC line.



In the early sections of this workbook I described loss of holding current, and triac shut-off due to the AC line current ringing below 0A. With the current and voltage probe in place, identify whether the triac is losing holding current, or AC line current is ringing below 0A.

- If the phase dimmer is losing holding current use the described method(s) within this document to increase the holding current at the point where the triac loses its holding current.
- If the current is ringing below 0A, use combination of resistor/capacitor snubbers to dampen the ringing. A good rule is to add (increase) differential mode inductance before you add EMI X-type capacitance. Also input series resistors with the line and neutral soften the inrush current. We believe you should use fixed values of resistors over NTC types so that the dimming performance is consistent over temperature.

LEDs Magazine Article on Optimizing SSL Bulb System Performance

design forum | ENERGY-EFFICIENT LED LAMPS

High LED drive currents with low stack voltages create efficiency challenges

The SSL industry is beginning to do a better job of optimizing the LED components, drive electronics, thermal design, and optical elements of a luminaire according to **MATTHEW REYNOLDS**, who details the energy-efficiency challenge.

SSL System Solution Success Story

Not long ago when I started developing LED drive solutions for solid State Lighting (SSL) systems there was a lot of buzz within the industry about "system level solution" design. This concept intended to integrate the design expertise (thermals, optics, LED, electronics) in order to create the best possible SSL solutions. By understanding all the design challenges a team of experts designing a system together had a better chance at creating an optimized SSL design than individual teams designing portions of the system in isolation. I really hadn't seen much progress with this type of collaboration until recently.

Background

Over the last ten years LED manufactures were increasing the efficacies of the LEDs at rapid pace. The industry recognized that increasing the efficacy of the LEDs was the single most important metric for SSL adoption. SSL solutions were not as cost effective as existing technologies, and the LED manufactures were focused on lumens per watt, or even better lumens per dollar.

The power electronics and IC manufactures had +30 years of experience with AC/DC and DC/DC voltage regulation topologies to draw from. Although the SSL lighting designs were unlike the voltage regulation applications, the technical learning's and power electronics manufacturing expertise were in place. LED driver topologies found in initial SSL products in the market were incremental improvements and modifications of existing voltage regulation schemes. AC/DC/LED drivers have unique requirements, and these requirements have reenergized a power electronics community to develop efficient, reliable and cost effective solutions targeted at the SSL driver market.

The primary and secondary optics of a SSL system is another piece of the system that needed performance and cost optimization. Although lumen loss due to secondary optics is minimal compared to the LED and the power electronics, it certainly needed improvements, and this industry was improving its processes.

SSL system cost, and how it shapes the design process

In order for SSL luminaries to attain mass adoption the end solutions needed to be cost competitive compared to incumbent light sources. LEDs are the most expensive component a SSL solution Bill of Materials (BOM). LEDs were manufactured on small wafer facilities that weren't yet optimized, and the sales of LEDs hadn't kicked in economies of scale. SSL luminary's manufactures realized that the easiest means to reduce system cost was to reduce the number of LEDs in the system. This further pushed the LED manufactures to create LEDs with greater efficacy numbers, and LEDs that had increased lumen output i.e. higher power LEDs.

The power electronics and power IC industry was very mature and their processes optimized, therefore only minimal cost savings would to be realized.

Energy Star Compliance effects on system development

Energy Star requirements were put in place to protect the consumer and ensure quality lighting products are being released into the market. One common Energy Star requirement is a minimum lumens/watt that the end product must meet. SSL retro-fit lamp replacement designs had lumen/watt requirements in the range of 40lu/W to 50lu/W. Certified Energy Star laboratories would run manufactures submitted products through a set of standardized procedures indicative of an end application of the product. Lumens would be measured, and input power recorded to come to an efficacy number.

All the pieces were in place to push the industry to mass adoption. The LED manufactures made amazing progress with the efficacy of the LEDs. The optics industry was minimizing the lumen losses and increasing the quality of their optics. The power electronics and IC manufactures were developing systems optimized for LED drivers, and all was good, or so we thought…

Cost vs Compliance (mutually exclusive directions)

A looming issue became apparent as soon as the luminary manufactures steadily decreased the number of LEDs need in a system, this was good for business, but created another technical challenge for the industry. It was first noticed in the A19/E27 lamp retro-fit market.

It was assumed that the LED driver would increase in efficiency, or at least remain similar to past designs as the number of LEDs reduced in the system and as the LEDs increased in lumen output. This was not being realized…What went wrong?

Typical SSL retro-fit bulb specification

60W incandescent SSL retro-fit bulb requirements:

- Input Voltage – 115VAC (+/- 20%)
- Output voltage – 10 LEDs in series (31V – 36V)
- Lumen output ~ 800 lumens
- LED forward current – 350mA
- Output power (max) – 12.6W
- Efficiency target – 85%
- FCC Class B
- UL8750 compliant
- Reliability > 50k-hrs
- System operating temperature 50°C

The trend today is to increase the forward LED current (higher power), and reduce the numbers of LEDs within the system. Expected specification to changes

- *Output voltage – 5 LEDs in series (15V – 17V)*
- *LED forward current – 700mA*
- *Lumen output ~ 800 lumens*
- *Output power (max) – 11.9W*
- Efficiency target – 85%

Although the output power reduced and the efficiency specification remained at 85%, one would expect greater lumens per watt number. In reality the efficiency of the converter dropped significantly, and hence the lumen per watt has decreased. What is even more alarming, is that the power dissipation within the circuit has increased, and caused design and reliability issues.

Energy Star compliance may be in question, and cost may be increased since the heat-sink, or potting material may now be required. What went wrong?

Review of Power Electronics power losses and efficiency

Losses within the power conversion stage can be categorized into three types.

1. Conduction losses
2. Switching losses
3. Quiescent losses

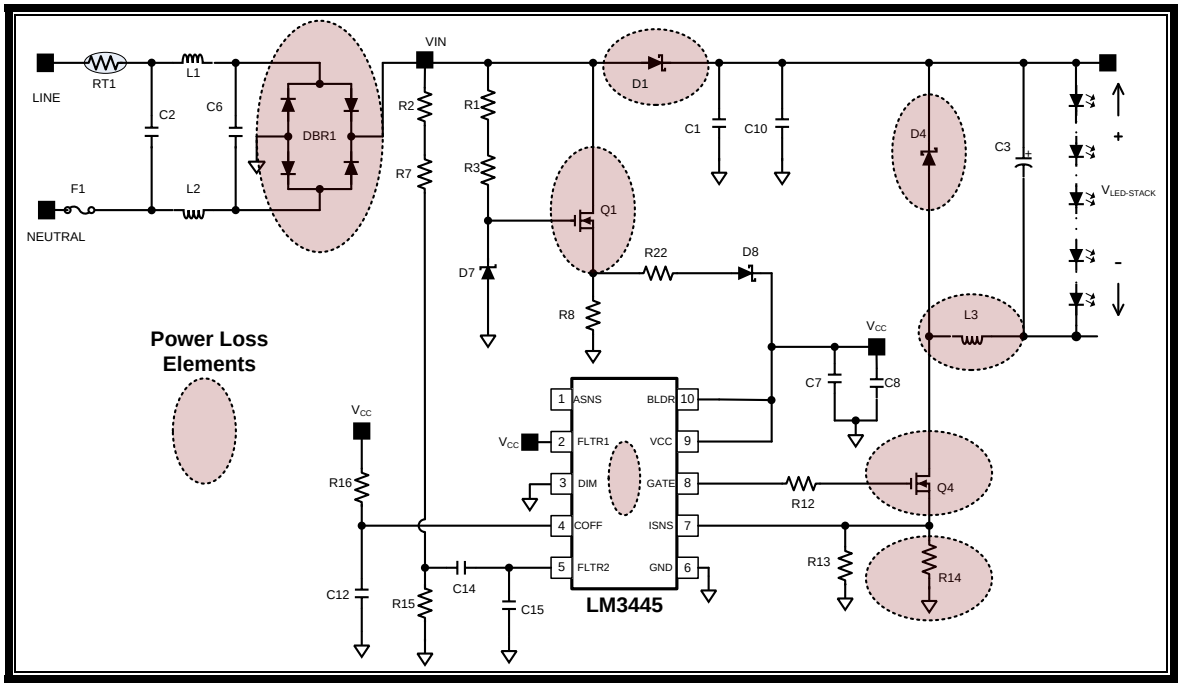
All silicon devices and passive components within a LED driver have resistance associated with them. Conduction of current through resistances results in I_{RMS}^2 x R power losses. Depending on the quality and type of components chosen (Mosfet, diode, magnetics) losses could vary as the system specification varies.

Switching losses occur during the transition from one Mosfet or diode being turned on while the other MosFET or diode is being turned off. A converter operating at 200 kHz will have twice as much switching loss than a converter operating at 100 kHz. A trade-off between operating switching frequency needs to be evaluated however. Switching at higher frequencies allows for lower inductance magnetic, and conduction losses may be reduced given fixed space requirements (lower R_{DCR}).

The quiescent power losses are associated with powering internal circuitry.

In summary - In similar LED driver designs, you may have the same output power ($P_{OUT} = I_{LED}$ X $V_{LED\text{-}Stack}$) but depending on the voltage, and currents of the system, and the type of components within the system efficiency of the system may vary wildly.

Typical Off-line (AC to I_{LED}) retro-fit SSL bulb circuit used in the optimization experiments



Definition of terms, and power loss calculations within the driver:

D = Duty-Cycle = $D \approx \frac{V_{LED\text{-}STACK}}{V_{IN}}$

D' = (1 - D)

F_{SW} = Switching Frequency

Switching losses when Q4 turns on → $P_{Q4\text{-}SW} = 1/2(V_{IN} \times I_{LED} \times F_{SW} \times T_{RISE})$

Q4 conduction losses → $P_{Q4\text{-}COND} = I_{LED}{}^2 \times R_{DSON} \times D$

D4 conduction losses are → $P_{D4\text{-}COND} = I_{LED} \times V_{DF} \times D'$

L3 Inductor conduction losses → $P_{L3\text{-}COND} = I_{LED}{}^2 \times R_{DCR}$

Now that all significant power losses have been calculated, we can solve for the overall efficiency.

Efficiency equals: $\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$

Where $P_{LOSS} = P_{Q4\text{-}SW} + P_{Q4\text{-}COND} + P_{D4\text{-}COND} + P_{L3-COND}$

Looking at the power dissipation equations one could quickly make some assumptions regarding stack voltages and currents in a SSL lighting application. By increasing the current through a reduced number of LEDs, the lumen output may meet specification, but efficiency will likely decrease. A detailed analysis should be completed to fully understand the design trade-offs and power losses, but a quick analysis makes the following points why the efficiency of the system dropped.

- The conduction losses in the inductor L3 will increase as the LED forward current increases.
- Switching losses in the free-wheeling diode increase if the LED forward current is increased
- By decreasing the stack voltage you have increased the percentage of time the free-wheeling diode D4 is conducting relative to the main switching MosFET is on. This HV diode will have larger conduction losses than the MosFET, and therefore power loss in the system has increased.
- Conduction losses will increase in the main switching Mosfet Q4 with increased LED current

Total system design, solving the problem

This article was written to increase awareness in the design community about SSL system level design. The specifications, cost, and performance are all variables to a successful design, and must be addressed as a system.

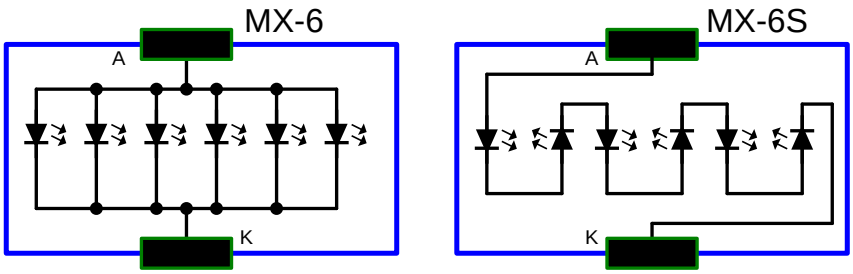
The power electronics community is developing LED driver solutions that are efficient and cost effective. This includes designs where the LED stack voltage is very small relative to the input voltage.

It was desirable for National Semiconductor to create LED drive electronics that would allow our customers to achieve Energy Star compliance. After analyzing many different types of LED and driver configurations in the laboratory it became apparent that the lower LED count with higher forward current would present an increased challenge to achieve Energy Star compliance for our customers.

The LED manufactures have also recognized that focusing on developing efficient single LEDs is not the whole story. LED manufactures need to be aware how their LEDs are being used in the market, and configure their LEDs to help optimize a specific SSL solution. LEDs used in retro-fit A19/PAR type lamps are very different than street-light, and MR16 applications. By working with design teams from other areas of expertise the LED manufactures have recently released LEDs specific to the end application.

System Level Success Story

LED manufactures have begun development of LED application specific products. One such product from CREE is the new MX-6S. The MX-6S LED is reconfigured from the older MX-6 LED, but this particular LED offers significant benefits if used in the right application, and in this case its benefits are recognized in retro-fit lamp applications. The original MX-6 LED has six LEDs in parallel within a single package. Each LED within the package would handle up to 150mA, for a total LED current of up to 1000mA. The LED had a forward voltage between 3.2V and 3.6V. The new MX-6S LED has the six internal LEDs configured in series. The forward current of the series string is up to 115mA. The single MX-6S package LED has a forward voltage between 19V and 22V. Simplified LED configurations within the packages are shown below.



The LED dice in both the MX-6 and MX-6S are identical as long as the binning, of the devices remains the same. The only difference between the two LEDs would be their internal bonding configuration. This single variable allowed for an excellent bench analysis between LED stack voltages in an A19 SSL lamp application with a common LED driver.

MX-6 vs MX-6S comparison bench analysis

The analysis between LED stack voltages and currents had the following goals and criteria:

- Optimize a common LED driver for common SSL retro-fit lamp applications with different LED configurations
- Record power loss and record critical component temperature
- Record any significant cost benefits with one design compared to the other
- Formulate driver and LED configuration recommendations with performance, cost reliability and manufacturability metrics in mind.

LED currents were adjusted to obtain a specific light output between the two designs using an inexpensive light measuring (flux) test system. This ensured us that relative performance was being compared, and took into account real system variables such as lumen loss due to temperature.

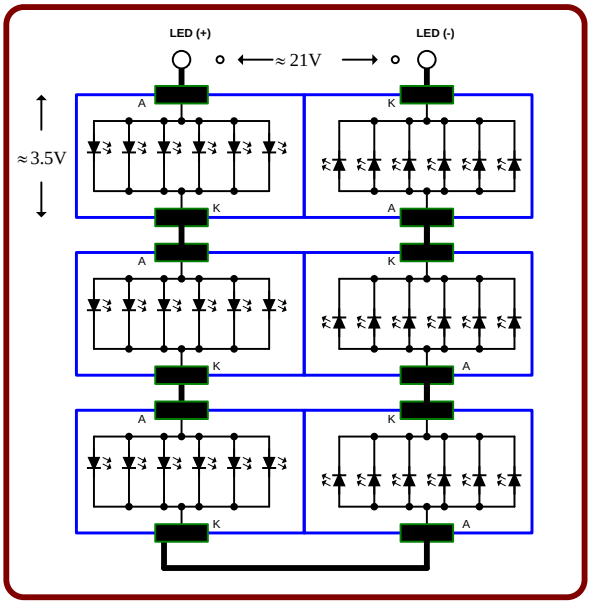
All variables were carefully controlled to minimize error. PAR Lamp used, light measuring set-up, measuring equipment, mechanical designs and heat-sinks, thermal equilibrium etc.

Empirical Analysis - low voltage vs high voltage LED stacks

60W Incandescent bulb to SSL Bulb design criteria

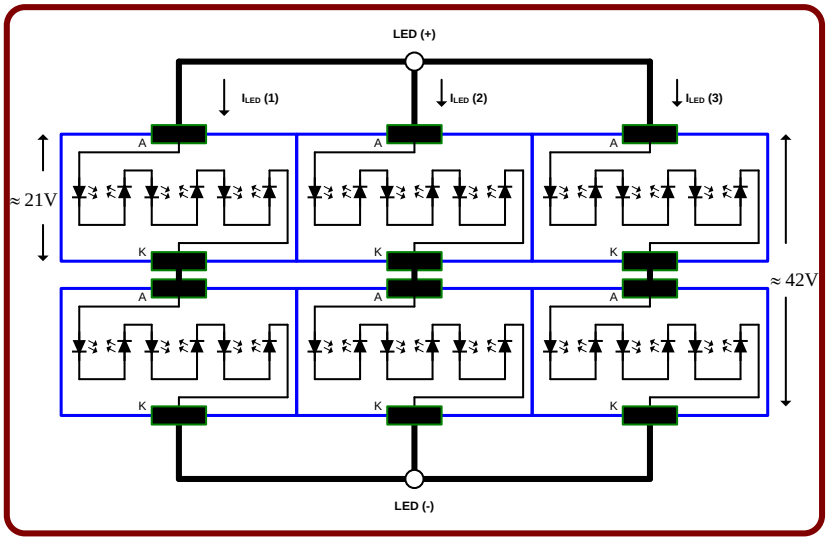
- V_{IN} 115VAC (+/-20%)
- PF > 0.70
- SSL Bulb lifetime > 30k-hours
- Reverse & Forward Phase dimmer compatible
- Dimming Ratio > 50:1
- 60W Incandescent equivalent (~ 800Lumens)

Design MX-6 – Six series MX-6 LEDs at 600mA - Each LED is ~133 lumens/w @ 600mA



# LEDs	I_{LED} (mA)	V_F LED	V_O	PO (W)	Eff (%)	Power Dissipation (W)
6	600mA	3.65	22	13.2	78.00	3.72

Design MX-6S – Six LEDs configured in a 3 X 2 array - total output current is 270mA, each string is 90mA. Each LED is ~133 lumens/w @ 90mA



# LEDs	I_{LED} (mA)	V_F LED	V_O	PO (W)	Eff (%)	Power Dissipation (W)
6	90mA X 3	21.25	42.5	11.5	86	1.75

Thermals Analysis and Reliability

MX-6 Analysis

The LED driver was placed in a plastic housing and inserted into a common PAR38 aluminum fixture. The driver and LEDs were assembled typical to a PAR38 retro-fit bulb solution. The design was first configured for six series connected MX-6 LEDs at 600mA. Thermocouples were attached to the electrolytic capacitor, main switching FET, main rectifier diode, and output inductor.

MX-6 Data

Input Voltage	LED stack Voltage	LED current	Efficiency
115VAC	21.6	600mA	78%
Thermocouple #	External Element	Temperature 20min	
1	Electrolytic Capacitor	65°C	
2	Main MosFET	100°C	
3	Inductor	101°C	
4	Output Diode	120°C	

MX6S Analysis

The same setup/bulb was used and reconfigured for six MX-6S LEDs.

MX6S Data

Input Voltage	LED stack Voltage	LED current	Efficiency
115VAC	40.15V	300mA	86%
Thermocouple #	**External Element**	**Temperature 30min**	
1	Electrolytic Capacitor	51°C	
2	Main MosFET	80°C	
3	Inductor	98°C	
4	Output Diode	90°C	

Conclusions and Recommendations

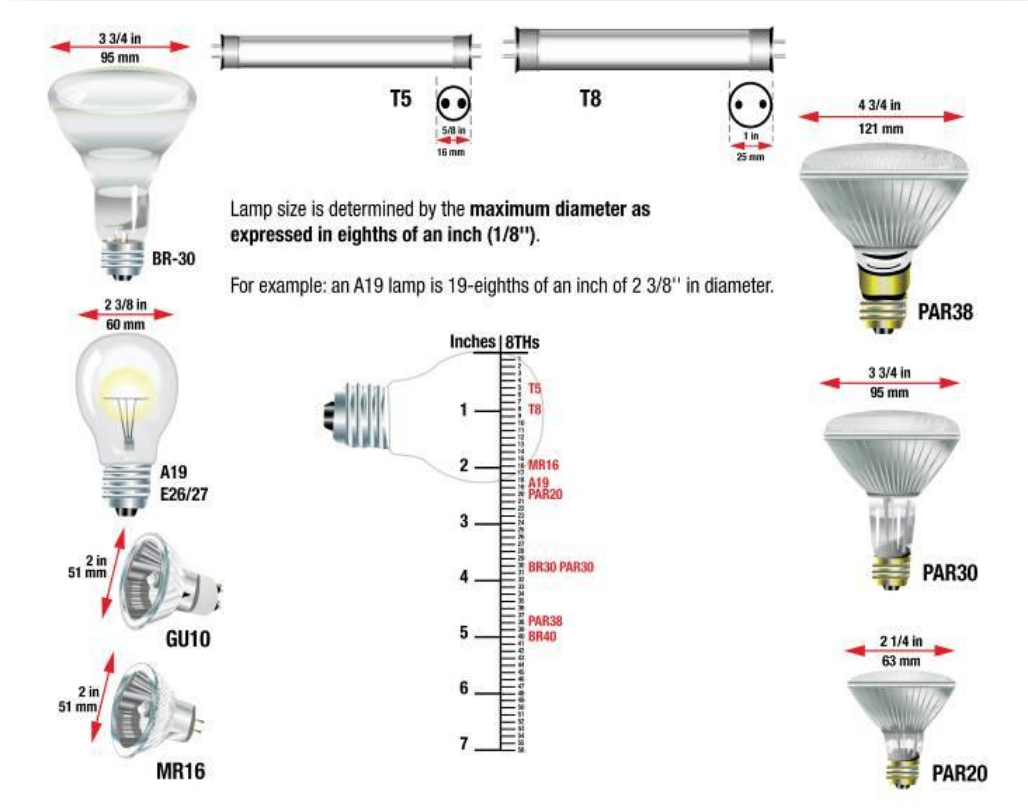
The item of most concern a systems design engineer should conclude from this simple analysis are the temperature differences of the critical components within the LED driver electronics between the two designs. This has little direct cost implications, but could be catastrophic to the manufacture due to returns, and a reputation for poor quality. Cost could be an indirect consequence if the manufacture was determined to use a particular LED configuration, and then was required to increase the efficiency with expensive drive electronics components, or was required to add additional heat-sink, or potting material to ensure the system components were within proper thermal specifications.

Often the electrolytic capacitor is the determining factor in the life expectancy of the drive electronics. If proper attention to design is taken, electrolytic capacitors can be used with confidence to gain +50k hours of life in SSL applications. A rule of thumb is that for every ten degrees Celsius you increase the temperature of an electrolytic capacitor, you half its life. As an example, if you were to use a 105°C 10k-hour rated electrolytic capacitor, you could expect at a temperature of 85°C, the capacitor would be considered good up to 40k-hours. If the same capacitor was operated at 95°C, the life expectancy would be about 20k-hours, a big difference. The difference in operational life of my application would at least double with the use of the higher voltage stack LEDs.

One detriment of the high voltage stack is the flexibility with the number o LEDs you might be able to configure in a system. In my example I wanted to limit the LED stack voltage to 52V, therefore only two MX-6S LEDs could be used in series. I therefore could only use even numbers of LEDs in my array (2X1, 2X2, 2X3, etc). CREE and Nichia offer a three series connected LED similar to the MX-6S, and this may increase the possible LED configurations.

SSL LED Bulb Information

Common Bulb Form Factors and Nomenclature



Light Output

Bulb Type	Traditional bulb "Power" Level	Type	Traditional bulb lumens	"Equivalent" LED power
A19	40W	Incand.	450	5-7W
	60W	Incand.	800	8-11W
MR16	35W	Halogen	400*	5-7W
	50W	Halogen	500*	6-8W
PAR38	60W	Halogen	1000*	14-18W
	120W	Halogen	1900*	25-30W
T8	15W	Fluorescent	900	10-13W
	30W	Fluorescent	2000	25-28W