Application Report
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PGA280 Communication via SPI™

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ABSTRACT

The PGA280 is a high-precision analog instrumentation amplifier that uses a serial peripheral interface (SPI) to control gain, the input multiplexer (MUX), several signal switches, the general-purpose input/output (GPIO) port, and a number of additional features. The PGA280 product data sheet provides a general description of the device register map and related functions. This application report offers additional descriptions and examples to explain how the PGA280 uses SPI communication protocols. For additional information about the PGA280, see the device data sheet (available for download at www.ti.com).

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1 Introduction

The PGA280 is a high-precision instrumentation amplifier with digitally-controllable gain and signal integrity test capability. This device offers low offset voltage, near-zero offset and gain drift, excellent linearity, and nearly no 1/f noise with superior common-mode and supply rejection to support high-resolution precision measurement. The 36V supply capability and wide, high-impedance input range comply with requirements for universal signal measurement. Special circuitry prevents inrush currents from MUX switching. In addition, the input switch matrix enables easy reconfiguration and system-level diagnostics—overload conditions are indicated. The configurable GPIO offers several control and communication features. The serial peripheral interface, or SPI™, can be expanded to communicate with more devices, supporting isolation with only four ISO couplers.

2 Conditions

The PGA280 reads data (on the SDI pin) with the falling edge of SCLK. DGND must be a stable potential within the supply range (normally GND; see the data sheet specifications), because the digital level translators distribute signals into the analog supply domain. The digital supply (DVDD) is normally connected to the main digital supply of the system, thus matching the logic levels of the SPI signals.

All examples in this document use hexadecimal notation, unless otherwise noted.

The example mnemonics that are sent denote the $\overline{CS}$ changing state by the capital letters ***L*** and ***H***: **L** indicates asserting $\overline{CS}$ = low, **H** represents asserting $\overline{CS}$ = high. All examples show hex values written to the register as required for the given example, but these values may be OR-combined with other bits that are required for other functions in the same register.

2.1 Digital Reset

The PGA280 performs an internal reset after power is applied to the digital supply DVDD (referred to DGND). The reset restores the default settings of the various device registers.

The digital supply (DVDD) can be turned on before or after the analog supplies are turned on.

There may be conditions where SPI signals are present first.If $\overline{CS}$ is high first, it pulls DVDD high via the input protection cell. As long as the supply voltage appears to be greater than 2.7V, proper device operation can be expected after DVDD turns on. However, depending on other loads on this supply, uncontrolled supply voltage conditions could prevent proper device reset. A software reset command (that is, a command that cycles $\overline{CS}$) helps to recover from such conditions, but proper and repeatable power-on conditions are recommended for reliable operation.

Software Reset Command, Register 1

```
L 41 01 H ;
```

Set $\overline{CS}$ = L, SDI data is 41 01, set $\overline{CS}$ = H

Alternatively, send the software reset command with a checksum byte:

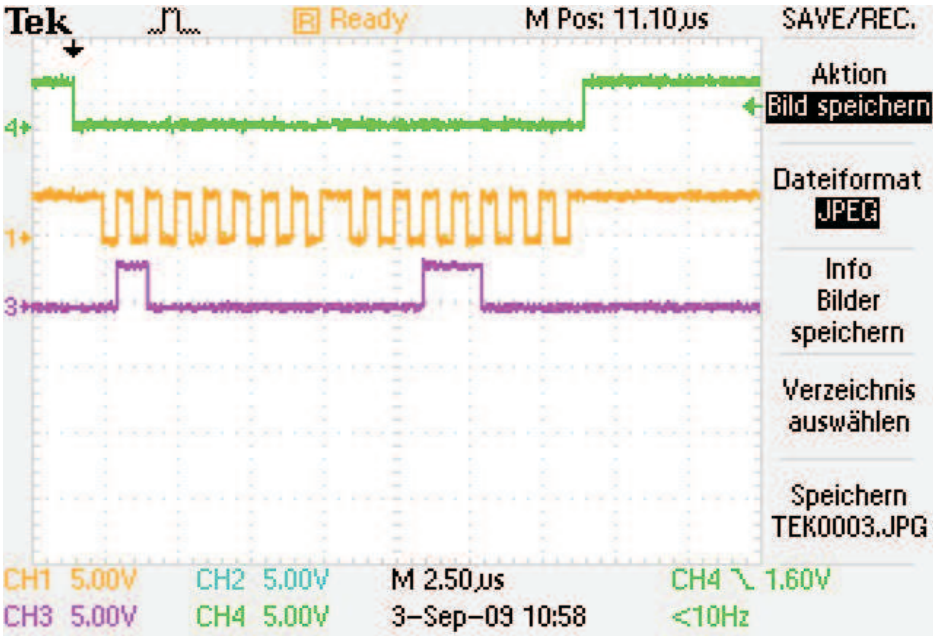
```
L 41 01 DD H ;
```

Set Gain

```
L 40 18 H ;
```

Sets a gain of 1V/V (18 sets the gain of 1V/V; see Table 2, *Input Stage Gain Settings* in the product data sheet)

Figure 1 shows a plot of the SPI waveforms that set a gain of 1. The PGA280 uses the falling edge of SCLK to detect the state of SDI.



- CH4: $\overline{CS}$
- CH1: SCLK
- CH3: SDI

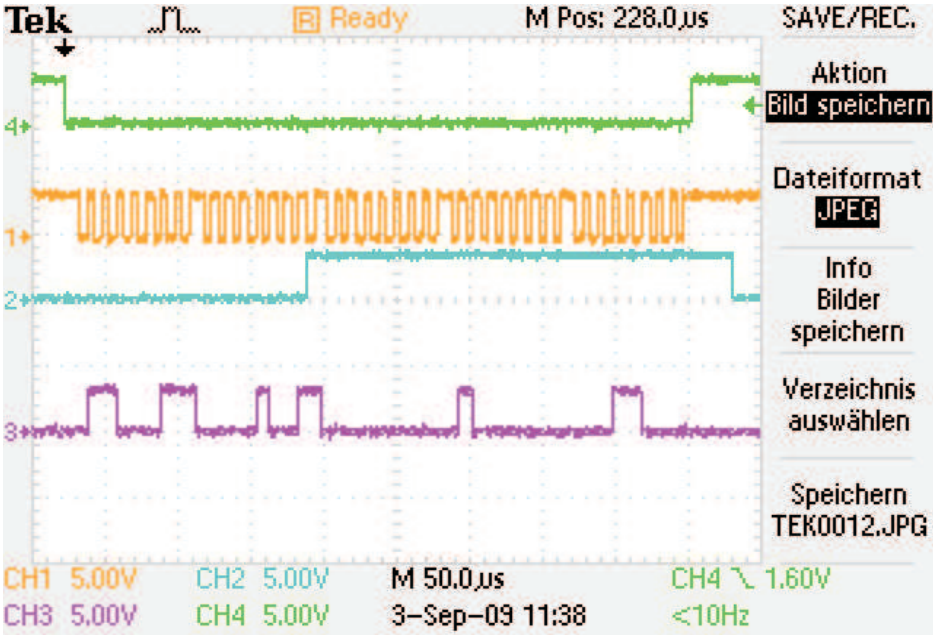
Figure 1. Set Gain to 1V/V

Gain is set to 1/8V/V (attenuation) after device reset. Changing the gain potentially overloads the input amplifier with a fast dynamic signal, especially with low gains and large signals. Therefore, it may be beneficial to activate the buffer (BUF) for approximately 36µs.

Changing the Gain to 1V/V with BUF

`L 63 09 00 40 18 H ;`	BUFTIM is set to approximately 36µs (0x09) together with the activation of BUF and the gain of 1V/V is set. The BUFTIM timeout (that is, the 36µs) starts ***after*** $\overline{CS}$ asserts H

Figure 2 shows how the *0x6309* instruction sets BUFTIM3 and BUFTIM0, and activates the BUF with the falling edge of the 16th clock pulse. Eight clock pulses follow as a dummy checksum byte. The *0x4018* writes to Register 0 and sets a gain of 1V/V.



- CH4: $\overline{CS}$
- CH1: SCLK
- CH2: BUFA
- CH3: SDI

Figure 2. Set Gain to 1V/V with BUF Activation

The BUFA signal returns to low after $\overline{CS}$ is asserted high, followed by the timeout of approximately 36µs.

Activate $BUFA_{OUT}$ to GPIO5

Figure 2 shows BUFA connected to GPIO5 in order to visualize the buffer timing. During design and timing evaluation, it is helpful to observe the buffer active timing cycle. In addition, this output could be used to trigger the analog-to-digital conversion.

`L 48 7F H ;`	Configure all GPIOs to output, or alternatively, use L 48 20 H
`L 4C 20 H ;`	Activate $BUFA_{OUT}$ to GPIO5; the buffer is active H by default

The *BUFA Timing* figure in the data sheet (Figure 55) and Figure 2 make use of this configuration. The bit BUFA Pol in Register 10 allows an inversion of the buffer active signal at GPIO5.

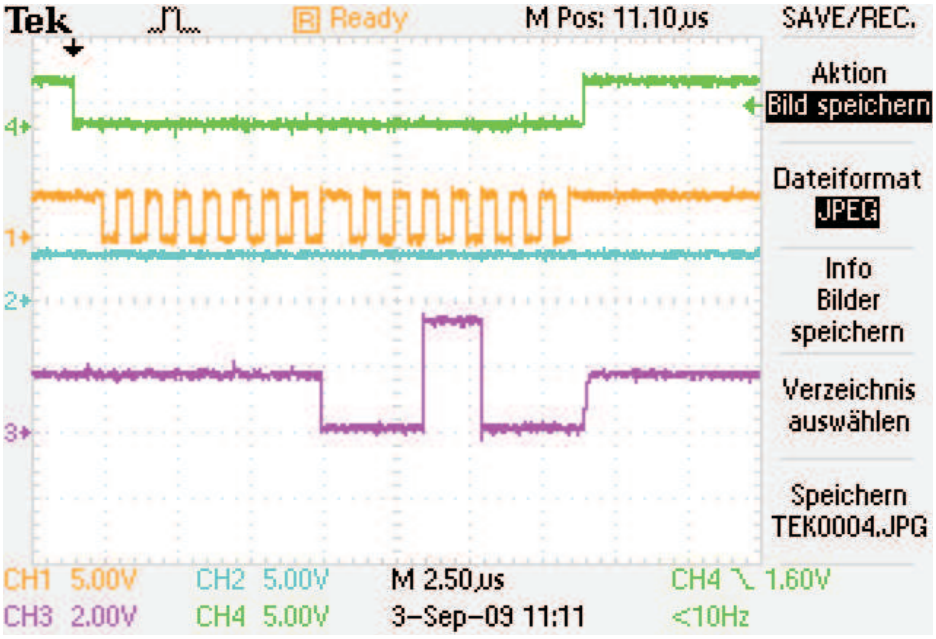
Read Register 3 (Test Read Operation)

Register 3 is set to *0x19* after a device reset. This command reads this value.

`L 83 00 H ;`	Send a read command to Register 3 and add eight extra cycles of SCLK

During these additional eight cycles of SCLK, the SDO pin sends *0x19* (it exits the 3-state mode during a sending data operation, and thereafter SDO returns to a 3-state condition). It would also send the CHKsum bit if 16 SCLK cycles are provided. Terminate the SDO to high or low, according to the specific system requirements.

As Figure 3 shows, SDO leaves the 3-state mode after the read command is decoded, and sends data during the following clock cycles. For a simple demonstration in this graph, SDO was terminated to the mid-supply of DVDD (3.3V) with 750Ω. Therefore, while in 3-state mode, the scope trace shows this mid-supply voltage. Asserting $\overline{CS}$ high terminates the transmission and sets SDO to 3-state mode again.



- CH4: $\overline{CS}$
- CH1: SCLK
- CH2: BUFA
- CH3: SDO

Figure 3. Test 3-State for SDO

SDO would transmit the checksum with eight additional clock pulses and then go to a 3-state mode automatically, even if $\overline{CS}$ is held low.

In general, SPI *reads* are very sensitive to data skew. The master detects the received data with its own clock. The slave device, however, may receive this clock as delayed, and as a result its data output (the SDO of the PGA280, also called *Slave Out Master In*, or *SOMI*) may even be delayed further. The reasons for this delay are logic gates or buffers and long wires. Isolation couplers, in particular, add a significant delay or data skew. Such delays or skew are often the reason for unstable communications; therefore, test the data patterns with a scope.

3 Internal Switches

The internal switches of the PGA280 are shown in the *Input Switch Diagram* (Figure 44) in the data sheet. After a device reset occurs, switches A1 and A2 (SW-A1 and SW-A2, respectively) are closed, routing the input signal from INP1 and INN1 to the amplifier input.

For using Channel 2, INP2 and INN2, send this instruction:

```
L 66 18 H ;
```

This command activates the BUF stage and connects INP2 and INN2 to the amplifier.

The fast switching from one input signal to the other would potentially generate a fast transient and dynamically overload the amplifier, but with the BUF already activated, the input clamp cannot draw current. Therefore, the input remains high impedance while the amplifier settles to the new value. The BUF turns off after a timeout according to register 3 (the default setting is approximately 100µs). This time can be reduced to approximately 39µs (that 4µs × 9 + delay) by writing:

```
L 43 09 H
```

4 Send Data to GPIO

The GPIO port can be initialized for either input or output for each individual port pin. After a device reset, all pins are configured as inputs. Reading Register 5 returns the momentary state at the pin. Open, unconnected pins return unpredictable information; therefore, terminate the device pins with resistors.

For output data to the pins, they must be assigned as *outputs*.

Each GPIO pin can be assigned as an output or input individually.

`L 45 03 H ;`	Load Register 5 (data) with 0x03
`L 48 7E H ;`	GPIO pins are set to output; only GPIO0 is an input. GPIO1 is set to H. GPIO0 ignores the Register 5 setting because it is configured as an input.
`L 85 00 H ;`	Read Register 5. SDO returns a byte with bit B1 = H and B0 indicating the state of the GPIO0 pin (external termination to H or L required).

When Register 5 is set before the GPIO direction is assigned, the state changes directly with assigning the role of *output* according to the contents of Register 5. Once configured as an output, data can be changed in Register 5 as required.

NOTE: GPIO pins are configured as *input* after a device reset; therefore, terminate all unused inputs or configure them as *output*.

WARNING

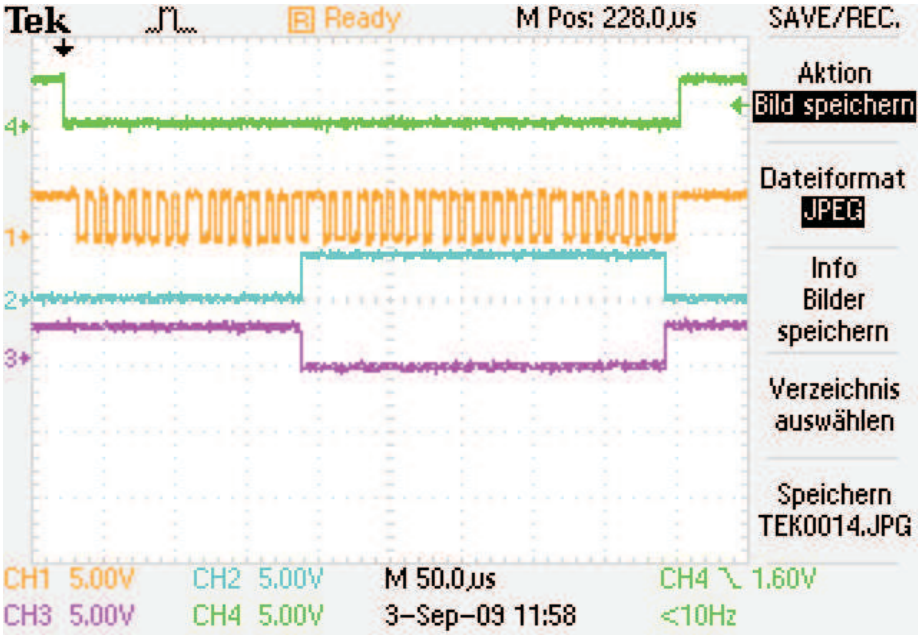
If GPIO outputs drive into a short, the current could be high enough to lower the digital supply voltage and consequently, disrupt communication; a locked condition may occur. Therefore, use resistors for termination.

GPIO pins can be toggled while $\overline{CS}$ low, but in this case the duration of the state directly depends on the SPI speed. The GPIO pin changes state directly with decoding of the command.

Figure 4 shows the sequence:

```
L 45 20 00 45 10 H ;
```

This sequence toggles the GPIO pins as indicated.



- CH4: $\overline{CS}$
- CH1: SCLK
- CH2: GPIO5
- CH3: GPIO4

Figure 4. GPIO Output

Read Error Status Register

The Error Status Register contains the individual flags being stored. Read Register 4 to detect the error flags. The bit B3, EF always turns on with any of the error flags. This bit is the OR combination of the individual errors and can be routed to GPIO3.

```
L 84 00 H ;
```

Read Register 4. SDO returns the contents of register 4.

Clear Error Flags in Error Status Register

After device power-on, depending on the power sequence and the state of the inputs, several error flags may be set. Therefore, clear this register after power-on occurs. After a readout of the register, it may be cleared. Furthermore, after setting up a new channel or gain, it may be useful to clear any existing errors.

```
L 44 FF H ;
```

Clear all error flags.

Individual error bits can be cleared by writing a '1' to the respective bit. Example:

```
L 44 04 H ;
```

Clear OUTerr (only)

Connect the OR Combination of the Error Flags to the GPIO3 Pin

GPIO3 can be assigned to the EF bit in Register 4 that allows a hardware indication of an error.

`L 45 00 H ;`	Sets all GPIOs to L state
`L 44 FF H ;`	Clear all error flags in Register 4
`L 48 7F H ;`	Assign all GPIOs to be outputs; all GPIO pins are low
`L 4C 08 H ;`	Assign GPIO3 to special function status, connecting the port pin to EFout in Register C

Now, GPIO3 would assert high as soon as an error appears. It remains high until the error is cleared in the Error Status Register (Register 4).

The latch condition for the errors can be disabled by writing:

`L 4B 90 H` (set LTD: Register 11, bit B7); see *Testing the Signal Path with a Scope Using the Error Flag (EFout) Output*.

With the latch disabled, the error duration can be observed at GPIO3 with a scope. The datasheet shows several examples: dynamic overload and signal overload.

Testing the Signal Path with a Scope Using the Error Flag (EFout) Output

`L 48 7F H ;`	Sets all GPIOs to output
`L 4C 08 H ;`	Activates EFout for GPIO3
`L 4B 90 H ;`	Sets LTD; error flags are not stored
`L 44 FF H ;`	Clears all error flags

Alternatively, use the combined string:

```
L 48 7F 00 4C 08 00 4B 90 00 44 FF 00 H
```

After this setup the error flag is only active while the error is present. This condition is indicated with the state of GPIO3 and can be observed with a scope.

In addition, Register 10 allows special settings. For example, writing *0x08* disables the error suppression while BUF is active; therefore, error conditions during a BUF active period can be observed.

A selection of errors can also be OR-combined to EF by using Register 10. Write a '1' to all errors that are to be suppressed.

5 Chip Select Mode for GPIO ($\overline{ECS}$)

The GPIO port can be used to generate $\overline{CS}$ for external devices. This $\overline{ECS}$ (that is, extended $\overline{CS}$) allows communication to additional devices by only using one SPI bus. The port activates the $\overline{ECS}$ after a one-byte command, and then ignores further communication until the $\overline{CS}$ to the PGA28 returns high.

To initialize $\overline{ECS}$:

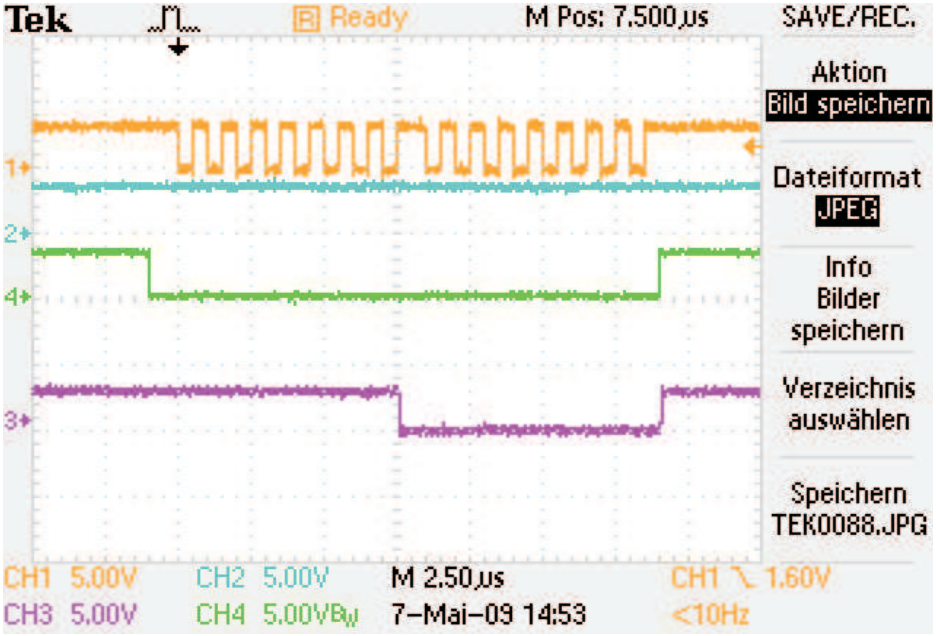
`L 45 FF H ;`	Set GPIO output data to H to avoid any glitches before $\overline{ECS}$ is assigned
`L 48 7F H ;`	Configure all GPIOs as outputs. Alternatively, configure only GPIO0 and GPIO1; send: `L 48 03 H`
`L 49 03 H ;`	Configure ECS0 and ECS1 as enabled in Register 9

Activate $\overline{ECS}$ ($\overline{ECS}$ is cleared when $\overline{CS}$ asserts H):

`L C0 00 H ;`	*0xC0* activates $\overline{ECS}$ to GPIO0

Just one byte (0x00) is sent for demonstration purposes; it can be many bytes (that is, there are no physical restrictions, only practical constraints).

Figure 5 shows the ECS signal (CH 3, or Channel 3). It asserts low with the last positive edge of SCLK and ends with the CS to the PGA280 (CH4). Here, just one byte was sent to the external device, but normally it would be as many bytes as needed for the communication to the device using ECS.



- CH1: SCLK
- CH2: SDO (not used)
- CH4: CS to PGA280
- CH3: ECS on GPIO0

Figure 5. ECS on GPIO0

Extended CS (ECS) uses a 1-byte command; therefore, ECS asserts low with the eighth clock pulse. With bit CP0 (clock polarity) set to '0', the ECS falls on the negative edge of the clock. If SP0 is set to '1' (in Register 2), it would fall with the previous rising edge. This approach allows the adaption of clock polarity to the requirements of the connected device.

Chip Select Mode (ECS) Using Checksum

To activate CHKsum:

`L 4B 11 F7 H ;`	Activates checksum, leaves FLGTIM as default (FLGTIM2 = 1)

A readback may verify the proper setting:

`L 8B 26 00 00 ;`	Read Register 11, reply on SDO. *0x1137*: Register 11 contains 0x11 (*0x37* is checksum)

Initialize ECS:

`L 45 FF DF H ;`	Set GPIO output data to H to avoid a glitch before ECS is assigned
`L 48 7F 62 H ;`	Configure all GPIOs as output.
`L 49 03 E7 H ;`	Configure ECS0 and ECS1 in Register 9

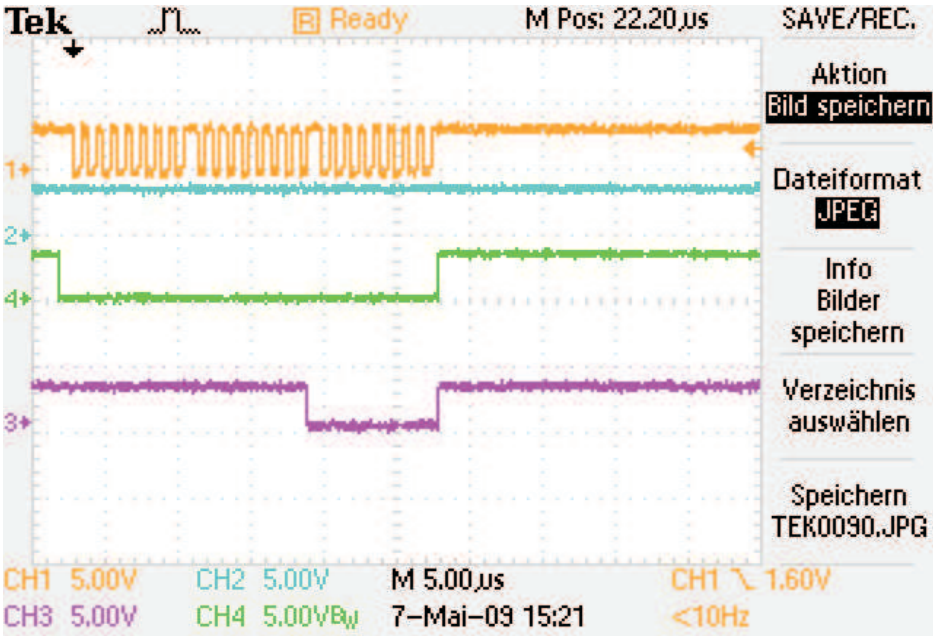
Activate:

```
L C0 5B 00 H ;
```

0xC0 activates ECS for GPIO0

Just one byte (0x00) is sent for demonstration purposes; it can be many bytes (that is, there are no physical restrictions, only practical constraints).

With CHKsum activated, the command for ECS is extended by the checksum byte, as Figure 6 shows. Therefore, ECS asserts low after the checksum is proven correct.



- CH1: SCLK
- CH2: SDO (not used)
- CH4: CS to PGA280
- CH3: ECS on GPIO0

Figure 6. ECS on GPIO0 in Checksum Mode

Checksum Incorrect or Missing

```
L 4B 01 H ;
```
Checksum is missing in this command

```
L 8B 26 00 00 ;
```
The reply from Register 11 is 0x0026***xx***.

The device has not entered checksum mode, because a proper CHKsum was missing. However, the register is set to 00, and thus FLAGTIM is set to 0x00. Note also that the last byte ***xx*** represents the state of SDO in 3-state mode; in non-checksum mode, the checksum byte of the command is ignored, and SDO starts sending data and default checksum with the 16 clock pulses after the command byte.

Write and Read Register 0 with CHKsum

```
L 40 18 F3 H ;
```
Set the gain to be 1V/V; therefore, write *0x18* to Register 0

```
L 80 1B H ;
```
Read Register 0:

```
0x1833 ;
```
18 was stored for gain 1 (0x33 is checksum)

Exit Checksum Mode

Setting bit B0 = 0 in Register 11 (CHKsumE) returns the SPI communication to non-checksum mode without changing or resetting the other register contents.

`L 8B 26 H ;`	Read Register 11 contents, AND content with *0xFE* (assumes a result of *0x10*, or default content).
`L 4B 10 F6 H ;`	Sends data to Register 11; Bit B0 = 0 = CHKsumE. From this point forward, checksum is no longer needed in communication.

6 MUX Control from Register 0

Register 0 is used to set the gain for the PGA280. But the last three bits also allow channel control for an external multiplexer. Therefore, writing to this one byte can switch the MUX channel and set the corresponding gain.

Multiplexed data acquisition must account for the fast signal transients that result from switching between channels. The PGA280 allows activation of the BUF with the command byte, and so the switching transient does not dynamically overload the amplifier nor reflect a current pulse into the signal source and signal filter.

These GPIO pins for MUX addressing change state according to the MUX2 to MUX0 bits *after* $\overline{CS}$ is asserted high. This combination, with the positive edge of $\overline{CS}$, ensures that the BUF can be active well before the transient appears, especially with fast SCLK rates. The BUFTIM setting also starts with $\overline{CS}$ high, and therefore its timeout covers the changes of the multiplexed signal until settled. The buffer timeout is set in Register 3.

Activate MUX Control from Bits B1 and B0 of Register 0 (CHKsum Not Active)

`L 48 FF 00 4C 07 H ;`	Set up GPIOs to all output mode and enable MUX0, MUX1, and MUX3

Set Gain and MUX Channel and Activate BUF

Example for MUX Channel 3 and gain 1V/V:

`L 60 1B 00 64 FF 00 80 00 H ;`	Set the gain to be 1V/V, activate BUF, and set MUX0 and MUX1 (MUX address 0x03)
`;`	Clear all error flags.
`;`	Read back Register 0

This is a typical command structure when scanning channels.

6.1 External BUF Control by GPIO4

The buffer (BUF) can be externally controlled using BUFTin. The BUF remains active with the external signal being high and times out after the external signal goes low. Using external BUF control requires a proper timing reference to switching transients. It may be used in systems that are controlled from microprocessors, where the BUFTIM delay setting is not sufficient because of unpredictable timing. It was originally intended for test purposes.

`L 48 6F 00 4C 30 H ;`	Sets all GPIOs to output except GPIO4, which is set to input. Register 12 activates BUFAout and BUFTin

This mnemonic activates BUFAout on GPIO5 and GPIO4 becomes the input-controlling BUF.

NOTE: Avoid overshoot of the control signal to achieve minimal distortion (that is, use series termination). The BUF active time can be tested at GPIO5 (BUFAout).

7 General Note

The PGA280 is a high-precision analog amplifier. The serial peripheral interface is a minimal communication bus to communicate to the register-controlled functions. It is recommended to avoid communication during a precise measurement in order to avoid coupled noise. The impact of such noise is difficult to predict, because it depends on layout, wave shape, and currents. Avoid large current loads to the GPIO and to the SDO.

The serial interface, in general, is sensitive to both data skew and delays; therefore, test signals for proper timing with a scope. Use the scope plots in this application report and in the product data sheet for reference.

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