BIG GIG REFERENCE PLATFORM

ADC08/500/D500/D1000/D1020/D1500/D1520

MANUFACTURING KIT / REFERENCE DESIGN (A1)

National Semiconductor GHz 8 bit ADC + XILINX Virtex 4

SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

National Semiconductor reserves the right to make changes to this product.
ALL parts labeled "N/A" are NOT ASSEMBLED.

Print Instructions:
- To create a readable printout, we recommend to use A3 or 11x17" paper size.
- When printing from this PDF file, make sure to check the "Shrink to fit" box.

SYSTEM CONFIGURATION

Module	Configuration	Description
FRONT END	2 channel DIFFERENTIAL	AC/ DC COUPLING ON I CHANNEL SIGNAL PATH. AC COUPLING ONLY ON Q CHANNEL SIGNAL PATH.
CLOCK SOURCE	DIFFERENTIAL	LMX231X PLL
FPGA		XC4VLX15 - 363 PIN BGA
USB I/F		CY7C64613 EZ USB

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PROJECT NAME:	BIG GIG REFERENCE BOARD REV. 2.0A				
DESIGNED:	IAN KING	DATE:	Oct 24th 2005	LAYOUT JOB#:	xx
DRAWN:	IAN KING/ C. CHASE	DATE:	May 9th 2006	LAYOUT REV:	REV 5.0
CHECKED:	-	DATE:	-	ASSEMBLY REV:	A1
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VCO and PLL Legend

BOARD	VCO	PLL
ADC08D15X0DEV, Rev. B	VCO190-1500TY	LMX2311USLDX
ADC08D10X0DEV, Rev. B	VCO190-992TY	LMX2312USLDX
ADC08D500DEV, Rev. B	VCO190-492TY	LMX2313USLDX

C1 100pF
C2 100pF
Y1 10MHz
R2 680
5VRF
R1 10
C159 470pF
C4 1uF
C3 470pF
5VRLY
C5 470pF
C6 100pF
R3 18
R4 270
R5 270
P4,5 SCLK
P4,5 SDATA
P5 PLL_LE
1V8IO
R6 10
R7 10K
U2 LMX231x (See Legend)
NC-3
Data
LE
GND
CE
Vuc
NC-4
CLOCK
FoLD
OSCout
NC-2
OSCin
Finb
Fin
GND
CPo
NC-1
VCC
FL
Vp
C9 100pF
C10 10n
C11 100pF
C12 1500pF
R8 10K
C8 27nF
R9 2K7
C13 470pF
R13 NA
U3 VCO190_xxxTY (See Legend)
GND-12
GND-11
VCC
GND-10
GND-1
Vt
GND-2
GND-3
GND-9
GND-8
RF_OUT
GND-7
GND-4
MOD
GND-5
GND-6
R147 18
R143 18
R144 18
C7 100pF
U1 RELAY-RF303
X2
X1
XA
C1
Y2
Y1
YA
C2
5VRF
3V3IO
R10 18
R12 18
C16 100pF
C17 10n
C18 100pF
C19 10n
T1 ADTL2-18
C14 4n7
C15 4n7
R14 N/A
CLKIN_P P4
CLKIN_N P4
EXTERNAL CLOCK INPUT
J3 SMA
Q1 BC817-25
P5 EXT_CLK_SELECT
R16 4.3K
R17 10K
R148 100K
R149 10K
R150 10K
Q8 BC817-25
P6,7,8 VIN
P3,6 5VRLY
P3,5,6,7,8 3V3IO
P3,5,7,8 1V8IO
P4 5VRF
U24 LP2986
GROUND
FEEDBACK
TAP
INPUT
SHDN
ERROR
SENSE
OUTPUT
L8 100MHz
C110 10uF
C111 10uF
C112 100n
CERAMIC ONLY

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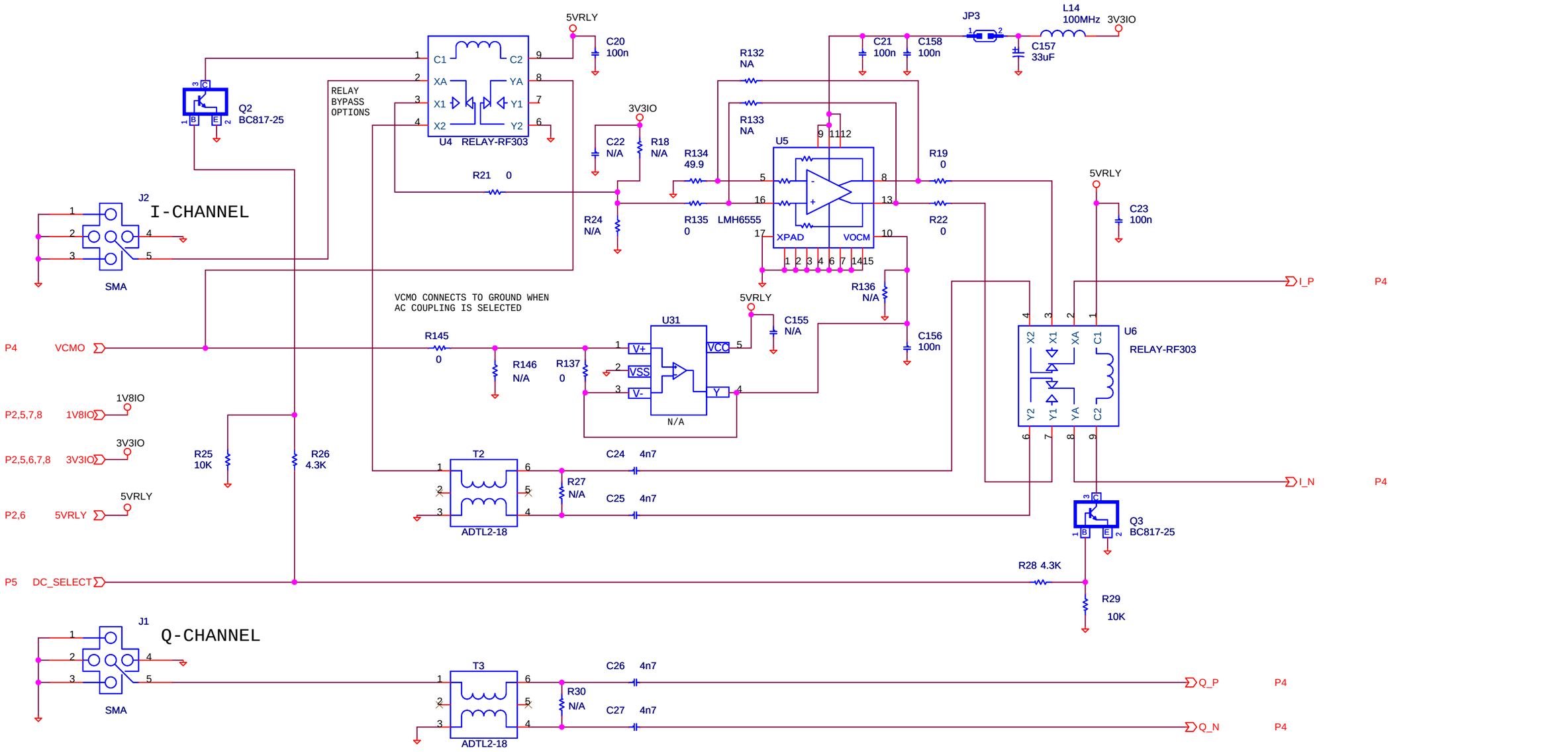

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U9D XC4VLX15_363FBGA

Note:
For ADC08D1X20, pin 41 on the chip itself must be either lifted or, preferably, entirely removed for the chip to function on this board.

5VRF
P2 5VRF

1V9
P6 1V9

2V5IO
P5,6,7 2V5IO

1.9V ADC SUPPLY MUST BE CONTROLLED BY FPGA SO THAT TRI STATE PINS ARE CONFIGURED CORRECTLY AT POWER UP

R38 N/A
R39 N/A
DCI RESISTORS FOR LVDS

R40 3K3
R41 3K3
R42 3K3
R43 3K3
R44 3K3
R45 3K3
R46 3K3
R47 3K3
R48 3K3
R49 3K3
R50 3K3
R139 N/A
TP2
TP SMD

P5 ADC_CS
P2,5 SCLK
P2,5 SDATA
P5 ECM_FSR
P8 DCLK_RESET
P5 POWER_DOWN
P5 POWER_DOWN_Q
P5 CALIBRATE

L1 100MHz
L15 100MHz
C30 22uF
C160 22uF
TP1
VCMO P3

U10
ADC081000_DUAL

P3 I_N
P3 I_P
P2 CLKIN_P
P2 CLKIN_N
P3 Q_P
P3 Q_N

C31 100n
C32 100n
C33 100n
C34 100n
C35 100n
C36 100n
C37 100n
C38 100n
C39 100n
C40 100n
C41 100n
C42 100n
C43 100n
C44 100n
C45 100n
C46 100n
C47 100n
C48 100n
C49 100n

C153 N/A
ADC_TD_N P5
ADC_TD_P P5

DCLK_P P5
DCLK_N P5
OVR_N P5
OVR_P P5

U30
TEST1P
TEST1N
TEST2P
TEST2N
R54 100
R63 100
2MM_7PIN_HEADER
test header

U33
TEST3P
TEST3N
TEST4P
TEST4N
R65 100
R68 100
2MM_7PIN_HEADER

U9E
XC4VLX15_363FBGA

R51 N/A
R52 N/A
DCI RESISTORS FOR LVDS

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PROJECT NAME: BIG GIG REFERENCE BOARD REV. 2.0A	PAGE TITLE ADC08D1000 VIRTEX 4 LVDS
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C50 100n C51 100n C52 100n C53 100n C54 100n C172 100n C173 100n C174 100n C175 100n

USB D- and D+ lines should be controlled impedance lines, as described in the Cypress document high_speed_usb_pcb_layout_recommendations_9.pdf

USB =>

EEPROM

U15 24C02/SO8

Cypress CY7C68013A-100AXC

TP_CY_CLK

CY_DATA[15:0]

JTAG HEADER

XC4VLX15_363FBGA

FIT IF CONFIG FLASH NOT INSTALLED

SDA/SCL - CROSSED WIRES - LIFT PINS AND FIX WITH WIRE MODIFICATION

TEMP SENSOR

LM95221CIMM

USB POWER ON & PB RESET

LM3722

DO NOT FIT V4 CONFIG FLASH IF CYPRESS USB CONTROLLER IS INSTALLED

XCF08P_VO48 N/A

100MHz FPGA CLOCK REF

PWR STB IDL CLK SMP OVR UPL TRG

LED_2x1

74LVC541

74LVC1G04

74LVC1G00

IDLE LED WILL ILLUMINMATE ONLY WHEN FPGA IS CONFIGURED

nPOWER_EN = 1 - SWITCH REGS SHUTDOWN (STANDBY)
nPOWER_EN = 0 - SWITCH REGS ARE ON

BANK1 - 1.8V IO

BANK2 - 3.3V CMOS

BANK3 - 2.5V LVDS

BANK4 - 3.3V CMOS

LVDS CLOCK AND OVER RANGE INPUTS FROM ADC

DCI RESISTORS FOR LVDS

Each unrouted FPGA pad should have a via connecting it to the bottom layer of the board. This will allow access to IO pins of the FPGA for development purposes.

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PAGE TITLE
USB CONTROLLER
V4 FLASH CONFIG
LED STATUS

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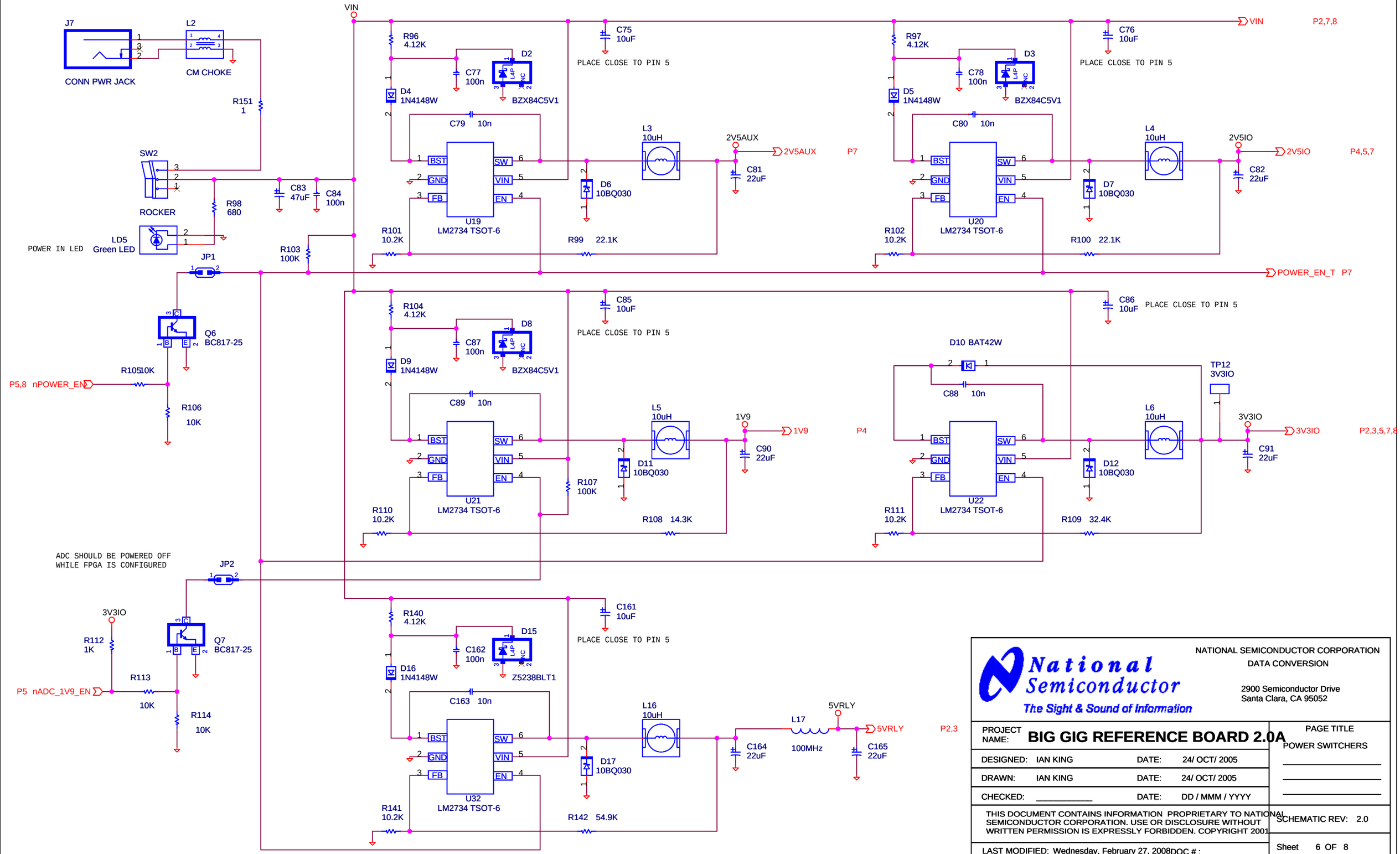

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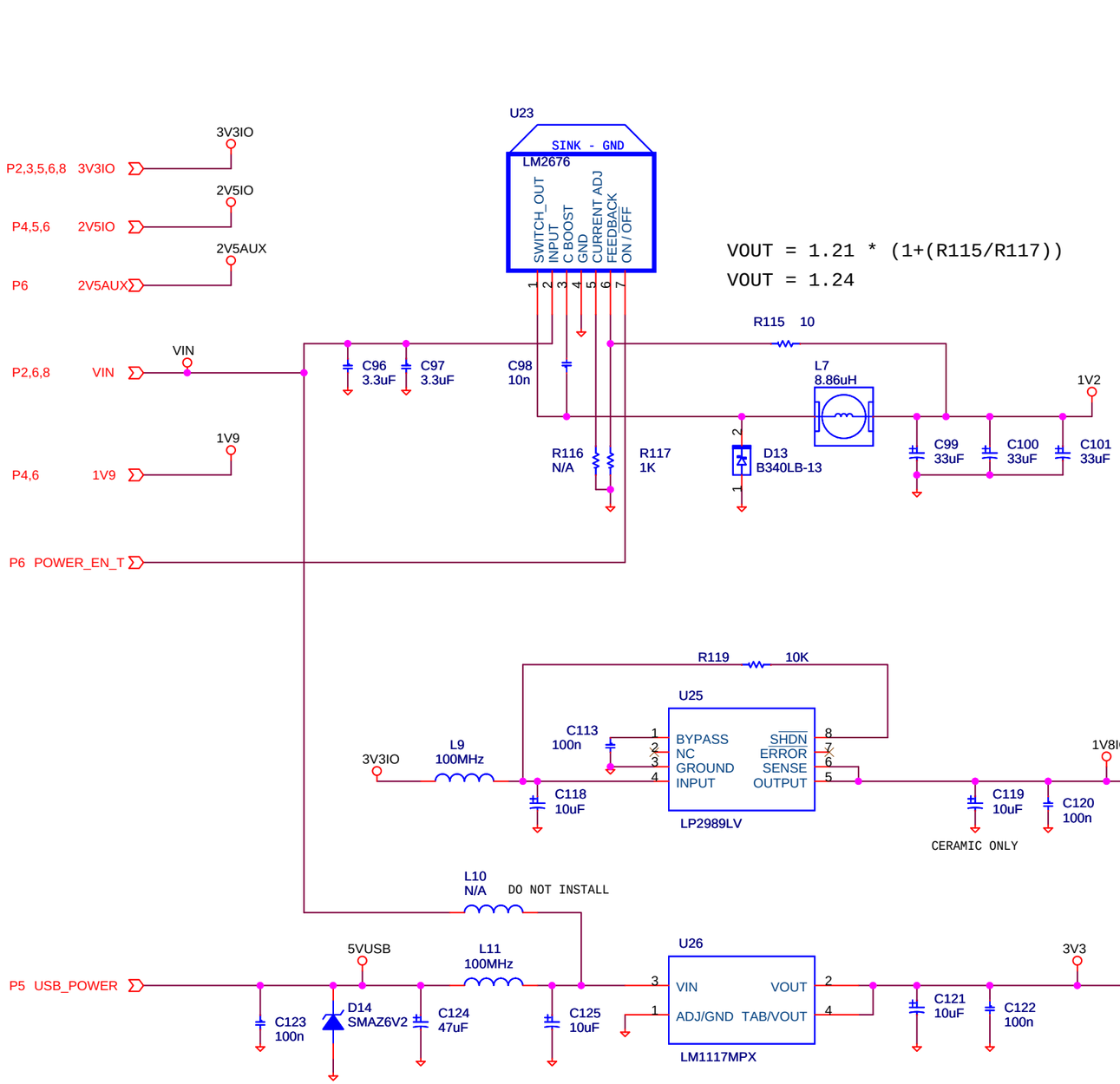
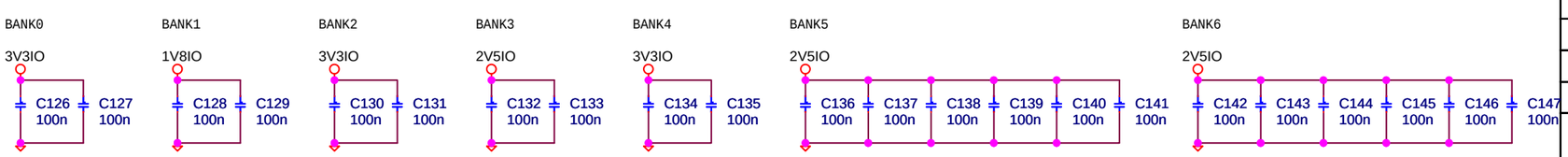


0402 FPGA Decouplers



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P5 SDA
P5 SCL
P5 MSTR_DATA
P5 MSTR_SCLK
P5 FPGA_RESET
P5 FIFO_FULL
P5 FIFO_EMPTY
P4 DCLK_RESET

1V8IO

U27
C148 100n
R129 47
READ P5
74LVC1G17

U28
C149 100n
R130 47
CAPTURE P5
74LVC1G17

P1 FUTUREBUS_24
SDA
SCL
MSTR_SDATA
MSTR_SCLK
FPGA_RESET
READ_IN
DATA_QA_P0
DATA_QA_P1
DATA_QA_P2
DATA_QA_P3
DATA_QA_P4
DATA_QA_P5
DATA_QA_N0
DATA_QA_N1
DATA_QA_N2
DATA_QA_N3
DATA_QA_N4
DATA_QA_N5

FUTURE BUS EXPANSION CONNECTOR

P2 FUTUREBUS_24
CAPTURE_IN
FIFO_FULL
FIFO_EMPTY
DCLK_RESET
DATA_QA_P6
DATA_QA_P7
STROBE_IP
DATA_QB_P0
DATA_QB_P1
DATA_QB_P2
DATA_QA_N6
DATA_QA_N7
STROBE_IN
DATA_QB_N0
DATA_QB_N1
DATA_QB_N2

P5 CONF_DONE
P5 V4_TMS

P3 FUTUREBUS_24
P5 V4_TCK
P5 V4_TDI
P5 V4_TDO
noISHUTDOWN
DATA_QB_P3
DATA_QB_P4
DATA_QB_P5
DATA_QB_P6
DATA_QB_P7
STROBE_QP
DATA_QB_N3
DATA_QB_N4
DATA_QB_N5
DATA_QB_N6
DATA_QB_N7
STROBE_QN

L12 3V3IO 100MHz
C150 100n
L13 VIN 100MHz
C151 100n

LOGIC ANALYSER HEADER

J8
+5V GND CLKe CLKo
D15e D15o D14e D14o D13e D13o D12e D12o D11e D11o D10e D10o D9e D9o D8e D8o D7e D7o D6e D6o D5e D5o D4e D4o D3e D3o D2e D2o D1e D1o D0e D0o
NC-1 NC-2 GND1 GND2 GND3 GND4 GND5
STROBE_QP
DATA_QB_P7 DATA_QB_P6 DATA_QB_P5 DATA_QB_P4 DATA_QB_P3 DATA_QB_P2 DATA_QB_P1 DATA_QB_P0 DATA_QA_P7 DATA_QA_P6 DATA_QA_P5 DATA_QA_P4 DATA_QA_P3 DATA_QA_P2 DATA_QA_P1 DATA_QA_P0
CONN 38 PIN MICTOR

U9F
IO_L25P_CC_SM7_LC_7 T17 STROBE_IP
IO_L25N_CC_SM7_LC_7 T18 STROBE_IN
IO_L26P_SM6_7 U18 DATA_QA_P1
IO_L26N_SM6_7 U19 DATA_QA_N1
IO_L27P_SM5_7 T15 DATA_QA_P7
IO_L27N_SM5_7 U15 DATA_QA_N7
IO_L28P_7 V19 DATA_QA_P2
IO_L28N_VREF_7 V20 DATA_QA_N2
IO_L29P_SM4_7 U16 DATA_QA_P6
IO_L29N_SM4_7 U17 DATA_QA_N6
IO_L30P_SM3_7 W18 DATA_QA_P3
IO_L30N_SM3_7 W19 DATA_QA_N3
IO_L31P_SM2_7 Y17 DATA_QA_P5
IO_L31N_SM2_7 W17 DATA_QA_N5
IO_L32P_SM1_7 V17 DATA_QA_P4
IO_L32N_SM1_7 V18 DATA_QA_N4
IO_L20P_7 R19 DATA_QA_P0
IO_L20N_VREF_7 R20 DATA_QA_N0
IO_L21P_7 R15 TP4
IO_L21N_7 R16 TP5
IO_L23P_VRN_7 T19 R120 51 VEXT
IO_L23N_VRP_7 T20 R121 51 VEXT
IO_L24P_CC_LC_7 R17
IO_L24N_CC_LC_7 R18
R138 10K
JP4
IO_L25P_CC_SM7_LC_8 U3
IO_L25N_CC_SM7_LC_8 U2 TP7
IO_L26P_8 T4 DATA_QB_P5
IO_L26N_8 T3 DATA_QB_N5
IO_L27P_8 T6 DATA_QB_P0
IO_L27N_8 U6 DATA_QB_N0
IO_L28P_8 V2 DATA_QB_P7
IO_L28N_VREF_8 V1 DATA_QB_N7
IO_L29P_8 U5 DATA_QB_P3
IO_L29N_8 U4 DATA_QB_N3
IO_L30P_8 W3 DATA_QB_P6
IO_L30N_8 W2 DATA_QB_N6
IO_L31P_8 Y4 DATA_QB_P2
IO_L31N_8 W4 DATA_QB_N2
IO_L32P_8 V4 DATA_QB_P4
IO_L32N_8 V3 DATA_QB_N4
IO_L20P_8 R2 STROBE_QP
IO_L20N_VREF_8 R1 STROBE_QN
IO_L21P_8 R6 DATA_QB_P1
IO_L21N_8 R5 DATA_QB_N1
IO_L23P_VRN_8 T2 R122 51 VEXT
IO_L23N_VRP_8 T1 R123 51
IO_L24P_CC_LC_8 R4
IO_L24N_CC_LC_8 R3
XC4VLX15_363FBGA

P7 VEXT
P2,6,7 VIN
P2,3,5,6,7 3V3IO
P2,3,5,7 1V8IO
P5,7 3V3

3V3 R124 10K
EXTERNAL STANDBY CONTROL
NOT REQUIRED IF USB MICRO IS INSTALLED
U29 74LVC1G06
3V3 C152 100n
3V3 R125 N/A
R126 N/A
nPOWER_EN P5,6

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