

A Guide to Voltage Translation With TXB-Type Translators

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ABSTRACT

Modern trends are driving the need for lower supply voltages across many system-level designs. As most processor voltage levels continue to decrease in the interest of achieving the lowest possible power consumption, peripheral devices maintain a need for higher voltage levels, creating potential for voltage discontinuities within a system. To remedy this mixed voltage system incompatibility, a voltage translator can be used.

Texas Instruments High Volume Linear group offers a wide range of voltage level translators. A variety of architectures provide solutions for different application environments including dual-supply direction-controlled, auto-direction sensing, and application-specific memory card interface translators.

The information in this application report is intended to help system designers understand the architecture and operation of the TXB-type auto-direction sensing translator family.

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1 The Need For Voltage-Level Translation

The need for voltage level translation is becoming increasingly significant in today's electronic systems. As the digital switching level standards have continued to progress toward lower voltage levels, system incompatibilities have arisen. [Figure 1](#) illustrates the trend toward lower system voltage levels and demonstrates the incompatibilities that mixed voltage systems can face.

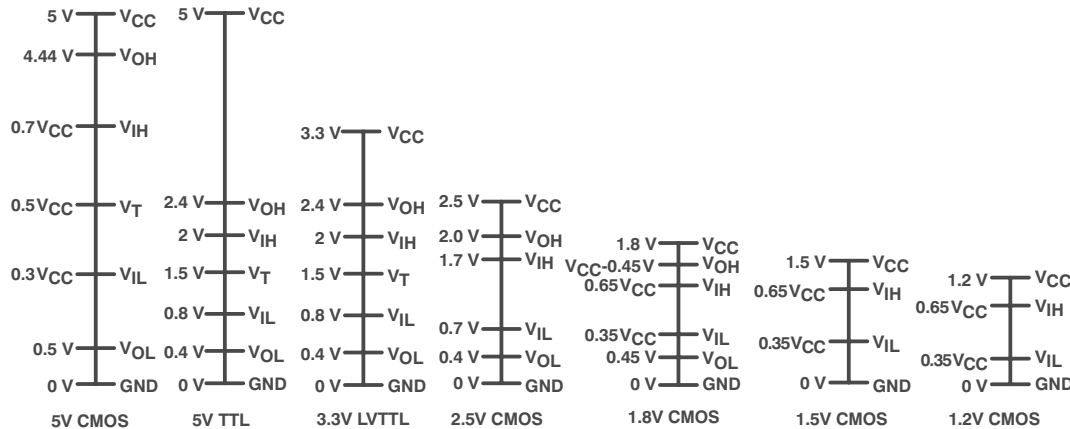


Figure 1. Digital Switching Levels

For two devices to interface reliably, the output driver voltages must be compatible with receiver input thresholds. For this condition to be met in mixed voltage systems, a voltage translator is often required.

Texas Instruments offers several unique device architectures for addressing voltage translation needs. The most familiar to system designers is probably a direction controlled buffer translator, such as the SN74AVC8T245. These translators can help remedy many problems in system voltage compatibility but do require DIR (direction) control pins. If the system environment does not provide a programmable GPIO to control the direction pin, an auto-direction sensing translator architecture can provide an alternative translation solution.

2 Auto-Direction Sensing Voltage Translator Architecture

If a processor GPIO input direction-control signal is not available or if one is not desired, an auto-direction sensing voltage translator can provide a robust solution. As the name implies, this type of translator does not require the use of a direction control signal, and each channel supports independent transmission or reception of data. This eliminates the need for a processor GPIO to control a DIR input, resulting in simplified software driver development as well as smaller device packaging due to reduced pin-count.

The TXB push-pull buffered type architecture does not require a DIR control signal to establish the direction of data flow. This architecture is designed to exclusively be connected and interfaced with a push-pull CMOS driver and is capable of driving a capacitive or high impedance loads in applications such as Secure Digital (SD) or Serial Peripheral Interface (SPI). The TXB010x devices are not intended for use in open-drain applications. For applications such as I²C where there is a need to connect and interface with an open-drain driver, TI offers TXS-type (i.e., "S" for Switch-type) translators. Please refer to TI application report, A Guide to Voltage Translation With TXS-Type Translators, literature number SCEA044 for more information on the TXS-type voltage translators.

[Figure 2](#) shows the basic architecture of a single-bit (or channel) of the TXB010x device.

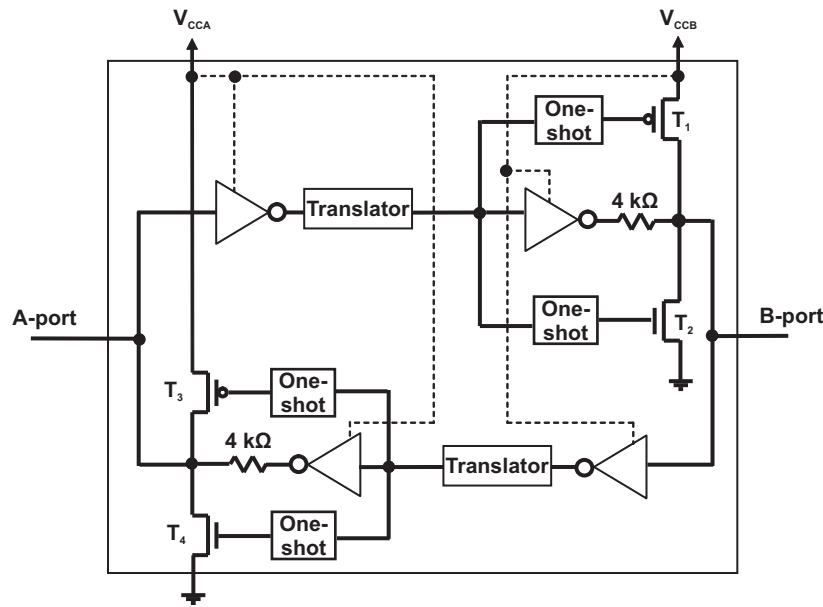


Figure 2. Basic TXB010x Architecture

The TXB translators incorporate a weak buffer with one-shot (O.S.) circuitry to improve switching speeds for rising and falling edges. When the A-port is connected to a system driver and driven high, the weak 4-kΩ buffer drives the B-port high in conjunction with the upper one shot, which becomes active when it senses a rising edge. The B-port is driven high by both the buffer and the T₁ PMOS, which lowers the output impedance seen on the B-port while the O.S. circuit is active. On the falling edge, the lower O.S. is triggered and the buffer, along with the T₂ NMOS, lowers the output impedance seen on the B-port while the O.S. circuit is operating and the output is driven low.

Figure 3 highlights with color the active circuitry involved in a low-to-high transition and a high-to-low transition. The weak buffer is shown in blue, and the active O.S. circuit is shown in green.

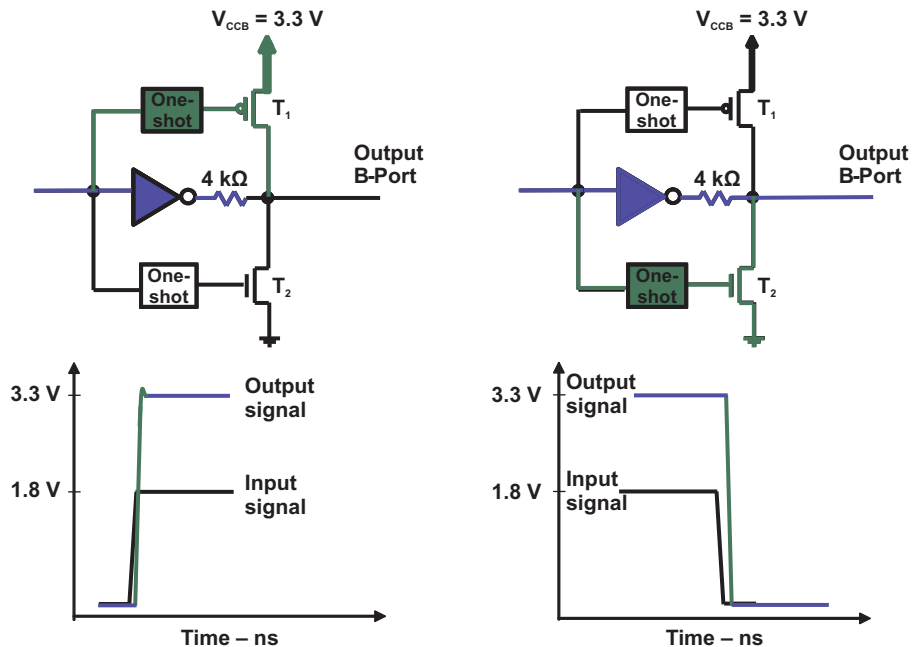


Figure 3. Active Output Rising/Falling Edge-Rate Acceleration Circuitry and DC Resistor Paths

The O.S. reduces the output impedance during the transition allowing the TXB device to drive a load while maintaining fast propagation delays and edge rates. Once the transition is completed, the O.S. circuit times out, and the buffer and the 4-k Ω pullup resistor hold the B-port signal high or low.

We call the TXB-type translator "weak-buffered", because it is strong enough to hold the output port high or low during a dc state, but weak in that the 4-k Ω impedance buffer can be easily over-driven by a system driver connected to the A or B port when a bus direction change is desired.

Figure 4 shows a typical I_{IN} vs V_{IN} curve.

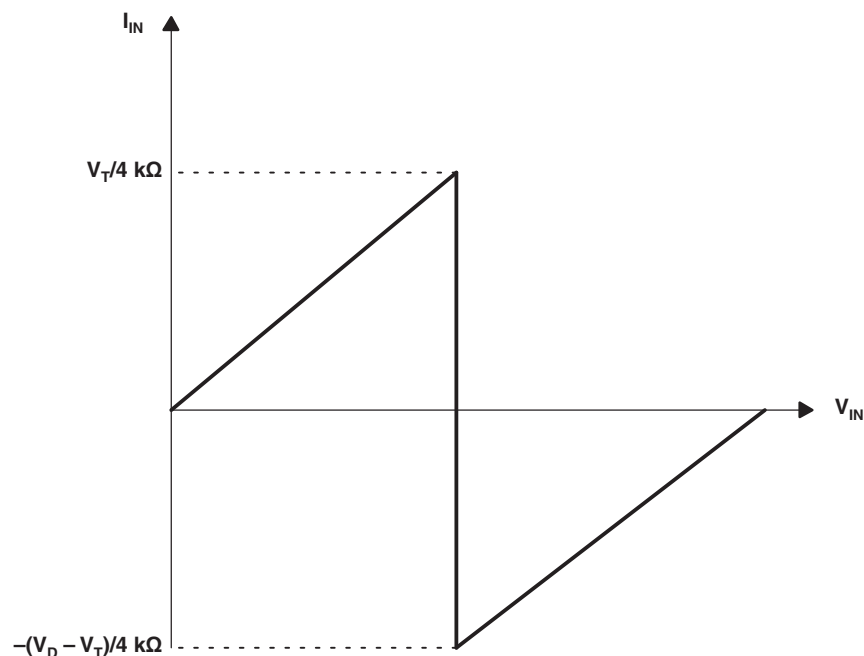


Figure 4. Typical I_{IN} vs V_{IN} Curve

Where,

V_T is the input threshold voltage of the TXB010x; V_T is typically $V_{CC1}/2$.

V_D is the supply voltage of the external system driver.

An external system driver must supply more than ± 2 mA of current to reliably overdrive the hold provided by the weak buffer.

3 Driving External Loads with TXB Translators

TXB devices were architected for driving high-impedance loads. If the application requires an external pull-up or pull-down resistor (R_{pu} or R_{pd}), special consideration must be given to the resistor value. When the output is in a steady high or low dc state, it is exclusively driven by the 4-k Ω impedance buffer. If an external resistor is added as either a pull-up or pull-down, a resistor divider network will be formed with the 4k Ω buffer. If the value of the resistor is too small, the V_{OH} or V_{OL} will be adversely impacted. If the value is large, (i.e. >50k Ω), there will be very little change in the output voltage level.

Equation 1 helps to illustrate how an external pull-up resistor affects the output V_{OL} levels. If an external 50-k Ω resistor is connected as a pull-up and the output is in a low signal state, then:

$$V_{OL} = \frac{4 \text{ k}\Omega}{50 \text{ k}\Omega + 4 \text{ k}\Omega} \times V_{CCO} = 0.075 \times V_{CCO} \tag{1}$$

As a result, if an external pull-up or pull-down resistor is needed, system designers should always choose large enough R_{pu} or R_{pd} values to ensure adequate V_{OH} and V_{OL} levels.

Figure 5 shows an illustration of a low-to-high, rising-edge signal for the TXB-type translators. The O.S. circuits turn on the PMOS transistor (T_1) for approximately 10 ns or 95% of the output edge, whichever occurs first. During this acceleration phase, the output resistance (R_{eff}) of the driver is decreased to approximately 40 Ω to 70 Ω to increase the current-drive capability of the device. When the circuits are active, a resulting high ac drive is realized by turning on T_1 and the rising-edge speeds up. The output port is maintained at a high signal level through this 4-k Ω internal resistor. With no load, the one-shots remain on for ~4.5 ns.

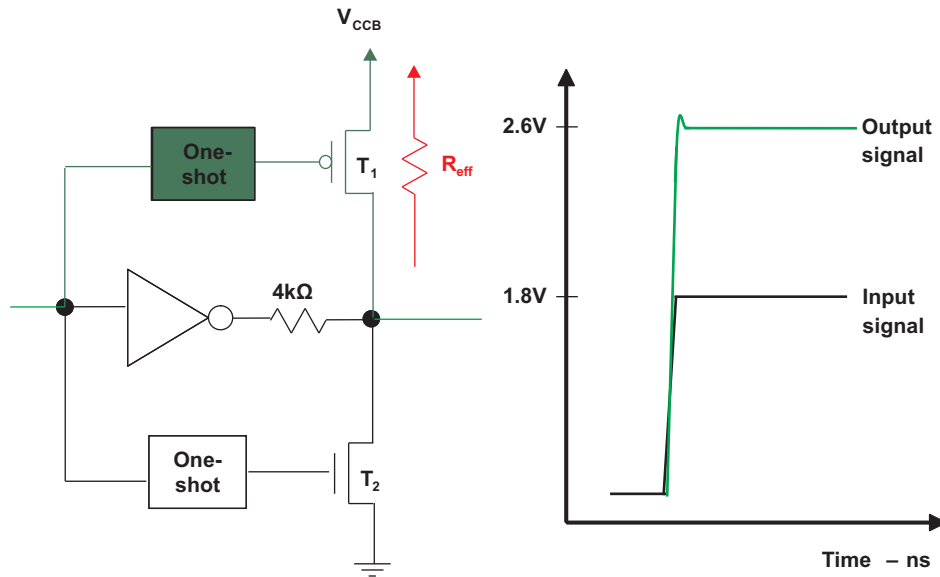


Figure 5. TXB Active Output Rising Edge-Rate Acceleration Illustration

During this ac drive acceleration period, the R_{eff} associated with the PMOS (T_1) and NMOS (T_2) is decreased to 40 Ω - 70 Ω . The typical output impedance varies based on output supply voltage, and is summarized in Table 1.

Table 1. TXB010x Effective Output Impedance Values

V_{CCO}	Output Impedance Value
1.2 V to 1.8 V	70 Ω
1.8 V to 3.3 V	50 Ω
3.3 V to 5 V	40 Ω

With regard to capacitive loads, TXB translators are designed to drive up to 70 pF without issue. If capacitive loading is larger than 70 pF, the O.S. will time-out after 10 ns and subsequently turn off before the output voltage is driven fully high or low. From there, the output will continue to rise or fall based on the RC time constant determined by the 4-k Ω buffer, load resistance and capacitive loading. To ensure reliable operation, system designers should keep capacitive loading for the TXB-type devices to 70 pF or less. With no external loading, the one-shot circuits will remain on for approximately 4.5 nsec. The duration of the one-shots is related to the output voltage level. The output high voltage at which O.S. switches off is approximately 95% of full scale, while the output low voltage at which O.S. switches off is approximately 5%.

4 Output Enable Control

The TXB devices offer low power consumption of 5- μ A maximum I_{CC} when the output enable is high. When the output enable is low, the TXB translator buffer will be disabled and the outputs are put into a high impedance state for increased power savings. The \overline{OE} input circuit is referenced to the V_{CCA} power-supply and when the device is disabled, the 4-k Ω buffer and the O.S. for both the A-port and B-Port are also disabled. In this state, output leakage (I_{OZ}) will be less than $\pm 2 \mu$ A. If the application does not require output enable control, The OE pin should be tied to the V_{CCA} supply. One should never leave the \overline{OE} pin floating in an indeterminate state as this can cause undesirable quiescent current to flow in the device, which subsequently increases its overall power dissipation.

Under partial power down conditions, the outputs are also disabled and put into a high-impedance state. This feature is referred to as V_{CC} isolation. If $V_{CCB} = 0$ V, the A-port is disabled. Likewise, if $V_{CCA} = 0$ V, the B-port will be disabled. In addition, the TXB type translators are fully specified for partial-power-down applications using the I_{OFF} feature. This I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when these devices are powered-down.

5 Conclusion

The TXB translators offer system designers a versatile solution for remedying mixed-voltage system incompatibilities. These translators eliminate the need for provisioning a processor GPIO, since they change the direction of the data flow automatically without the use of a direction control pin. This simplifies system level design and allows for solutions in smaller packages.

Please visit www.ti.com for data sheets and additional information on all bit-width TXB translators along with the full line of Texas Instruments voltage-level translators.

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