

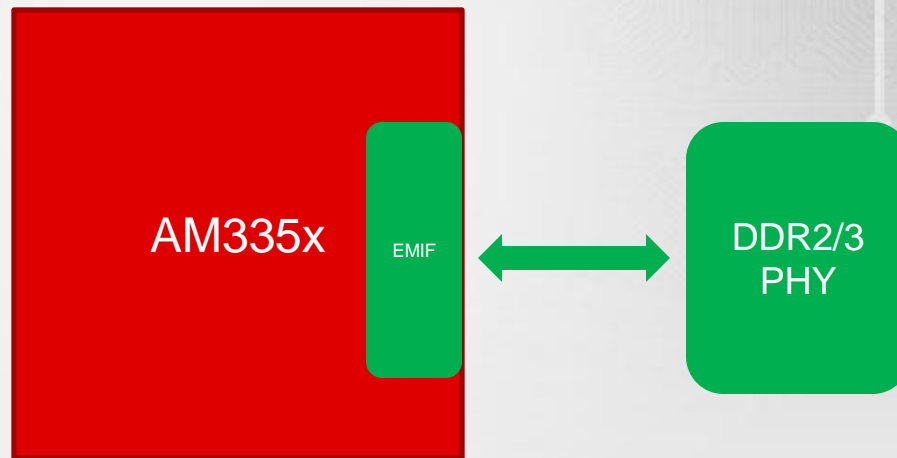
TI Sitara AM335x DDR3 Configuration & Software leveling

刘靖伟

Steven Liu

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DDR3 Configuration

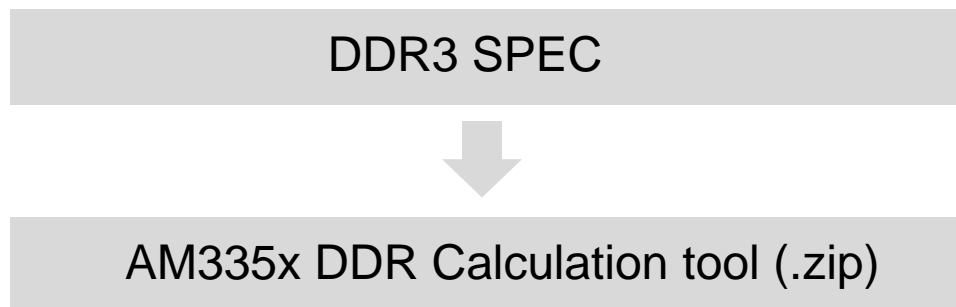


DDR3 Configuration

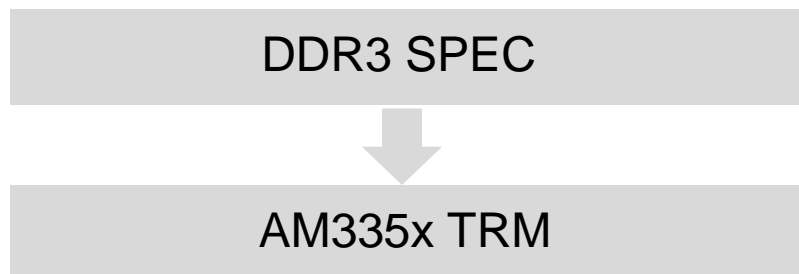
1. EMIF的配置

特别强调：确认DDR的型号（丝印）；正确完整的DDR3手册！

a. TIMING1,2,3 的配置



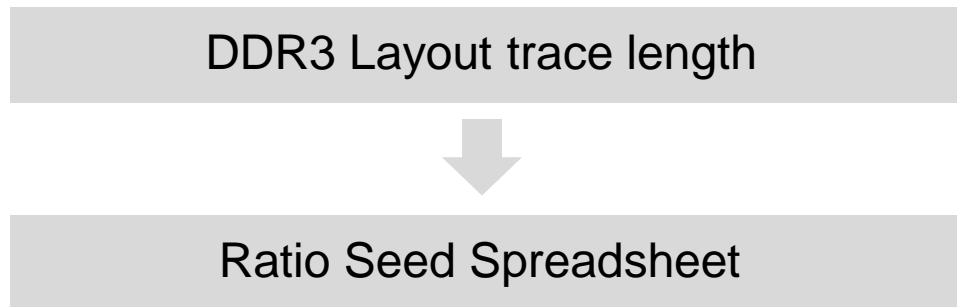
b. SDRAM_CONFIG 的配置



参考：http://processors.wiki.ti.com/index.php/AM335x_EMIF_Configuration_tips

DDR3 Configuration

2. Ratio Seed 的配置



特别强调：在量DDR_CK，DQS走线的时候，不要把匹配电阻的走线算在其中，只算从335芯片的pin脚到DDR3的pin脚间的走线长度！

参考：

http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling

DDR3 Configuration

3. DDR3 Software Leveling

a. JTAG口

- i. JTAG接口. 14 Pin 或者20 Pin。
- ii. 仿真器. 比如XDS100v2
- iii. 初始化板子的GEL文件!
- iv. 算法文件: `DDR3_slave_ratio_search_auto`

特别强调：要根据前面结果修改GEL DDR3配置！

参考：

http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling

b. SD卡

- i. SD卡启动
- ii. 需要有串口0作为调试信息输入输出。
- iii. 算法MLO文件。

参考：

https://www.deyisupport.com/question_answer/dsp_arm/sitara_arm/f/25/t/53263.aspx

Example



Example Configuration

样机上所用的是美光 DDR3 ，

样品上的丝印信息为：5YK77 D9PSK

MT41K128M16JT-125 IT:K

Specs

Orderable Parts for: MT41K128M16JT-125 IT

[SEE ALL DDR3 SDRAM PARTS](#)

	Status	Media	FBGA Code	SPD Data	Chipset Validation	PLP	Start Date	Alternative Part
MT41K128M16JT-125 IT:K	Production	N/A	D9PSK	N/A	N/A	No		N/A

Detailed Specifications

Density	2Gb	Part Status	Production	RoHS	Yes	Depth	128Mb
Width	x16	Voltage	1.35V	Package	FBGA	Pin Count	96-ball
Clock Rate	800 MHz	Cycle Time	1.25ns	Op. Temp.	-40C to +95C	CL	CL = 11
Data Rate	DDR3-1600	Features					

Example Configuration

DDR3L SDRAM

MT41K512M4 – 64 Meg x 4 x 8 banks

MT41K256M8 – 32 Meg x 8 x 8 banks

MT41K128M16 – 16 Meg x 16 x 8 banks

- Timing – cycle time

– 1.07ns @ CL = 13 (DDR3-1866) -107

– 1.25ns @ CL = 11 (DDR3-1600) -125

128 Meg x 16
16 Meg x 16 x 8 banks
8K
16K A[13:0]
8 BA[2:0]
1K A[9:0]

Table 73: DDR3L-1600 Speed Bins

DDR3L-1600 Speed Bin		-125 ¹		Unit	Notes	
CL- ^t RCD- ^t RP		11-11-11				
Parameter	Symbol	Min	Max			
Internal READ command to first data	^t AA	13.75	–	ns		
ACTIVATE to internal READ or WRITE delay time	^t RCD	13.75	–	ns		
PRECHARGE command period	^t RP	13.75	–	ns		
ACTIVATE-to-ACTIVATE or REFRESH command period	^t RC	48.75	–	ns		
ACTIVATE-to-PRECHARGE command period	^t RAS	35	9 x ^t REFI	ns	2	
CL = 5	CWL = 5	^t CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8	^t CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	ns	3
	CWL = 6	^t CK (AVG)	Reserved		ns	4
	CWL = 7, 8	^t CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5	^t CK (AVG)	Reserved		ns	4
	CWL = 6	^t CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^t CK (AVG)	Reserved		ns	4
	CWL = 8	^t CK (AVG)	Reserved		ns	4

视频地址

TI Sitara AM335x DDR3配置讲解:

http://v.youku.com/v_show/id_XMTY1NzE2NjY1Ng==.html

TI Sitara AM335x DDR3配置实例讲解:

http://v.youku.com/v_show/id_XMTY1NzE4ODUwNA==.html

THANKS